Project Technical Report

Design of Digital Controller Power Supplies at Yerevan Physics Institute

Part I

(From January 2004 to January 2005 for 12 months)

Yerevan Physics Institute

November 2004

This work is supported by DESY under the "Collaboration Agreement between DESY and YerPhI" (Attachment 1 to Appendix 3).

Introduction

The objective of this Project is to design and development of the new modern switch-mode power supplies at Yerevan Physics Institute to be used in the accelerator power supply systems at DESY (PETRA, X-FEL).
According to the collaboration Agreement in the first-year period the following volume of the work has been carried out:

- Study of the new switch-mode power supplies and new technologies used in design of power supplies digital subsystems.
- Building of the test stand of power-supply system to test digital control board and software.
- Development of digital control board using FPGA from Altera and test of the Chopper Interlock program.
- Working-out of the technical documentation.

To the end of 2004 will be completed development of the controller with FPGA and its integration in the power supply system.
The prototype control board including documentation will be sent to DESY.
The quarterly progress reports have been submitted.

On the next stage (from Jan 2005 to Jan 2006) the following will be done:

- Connecting FPGA power supply controller and Intelligent Internet based controller.
- Incorporating remote control for the power supply using a DESY standard control system.
- YerPhI sends the digital power supply control board and the documentation to DESY. MKK incorporates the digital control board to a switch-mode power converter and connects it to the machine control system.

POWER SUPPLY TEST STAND

Introduction

For the investigation of Chopper control system there has been built test-stand with experimental device, which is basically a logical board, processing input signals. Objectives of this work are

- To study new technologies on the basis of PLD (Programmable Logic Device) and
- To replace old logic devices with up-to-date digital devices

Device consists of hardware and software. For hardware there is an experimental electronic board. Software is realized into FPGA (Field Programmable Gate Array) EP1K00QC208-1, series of ACEX1K, Altera co.

Programme Modules

Programme part can be divided into few programme modules.

1. Main Interlock programme, which implements all main logic of block system
2. Reset program
3. Programme for external devices and test of lamps.

All these programmes operate independently and can complement each other. The main Interlock program operates permanently, and test of lamps is activated, when power is supplied on Altera chip. After power is supplied, signal with logical value HIGH appears on all inputs, and all LED signal unless they are out of order.
The programme for external devices provides control and blocking + 24V preventing the main Rectifier contaktor from switching on.

Interlock Programme

The main Logic of Interlock is realized on this Programme. It processes all Interlock signals coming from Chopper, Electronics, DCCT and external devices. Programme input signals are formed from

a) Chopper
   - ELS (Electrical Protection at the MOSFET)
   - UTR (Driver UnderVoltage)
   - UT (Overtemperature Chopper)

b) Electronics (Regulator)
   - UMIN (UnderVoltage for Rectifier)
   - UEA (OverCurrent)

- UHB (AuxiliaryVoltage (± 15V, 5V))
- OLN (Overload Negative)
- OLP (Overload Positive)

c) DCCT and external devices
- DCCT (DCCT Ready)
- DWW (Waterflow)
- MST (Magnet Steuerung)
- Personnel (Protection)

The programme output signals are

- Zpein (Enable for Pulse Gate)
- Turn Off PS (Enable for Power Supply)
- Beam InHibit (Enable for Damp)

Software Description

As have been mentioned above Interlock programme starts working after receiving Reset signal. For giving Reset signal there is a button "RES" on the front panel (Sheet 5, Switch 1). After indication of signal "RES" the programme starts processing signals coming from devices on its inputs.
If all devices work properly, all Interlock signals formed by them will have logical value LOW. The programme, processing these input signals forms output signal ZPein, which will have logical value HIGH (Sheet 8,Fig. 2). This signal opens optocoupler (IC03-A, Sheet 5), and voltage appears on the coil of relay KT8 (Electronic). Closed contact of this relay (KT8) allows control signals (Pulse Gate) to triggering the transistor (MOSFET).
In case of any failure in devices signal ZPein gets value LOW and blocks Pulse Gate.
The following reasons may cause blocking of Puls Gate:
- Low voltage of the main device (Rectifier), UMIN is activated
- Overcurrent Protection, UEA is activated
- DCCT does not work or is faulty
- Voltage of micro-schemes (±15V, 5V) does not correspond to nominal value
- Temperature Protection,UT is activated
- UnderVoltage for MOSFET driver is activated
- Overload (OLN or OLP) is activated

In case of ELS signal fault Pulse Gate is blocked first, then Rectifier is switched off (Sheet 9).
The same process is taking place, if there is a defect in the water-cooling system. For excluding false activations occurring from the nature of water flow, blocking is taking place, if duration of the signal DWW is few seconds (in our case it's ≤ 2 sec.)
In these cases the programme forms output signal "Turn Off PS", which blocks Rectifier through optocoupler (IC 04 –A, Sheet 5).

All such failures are indicated by control lamps signals; any faults are visually displayed on the front panel. After elimination of defects a special logical programme (for avoiding operation in unstable condition) is used to prevent Pulse Gate from unblocking until signal "RES" is given.
(Sheet 8, Fig. 1).
The programme also allows manual blocking of ZPein with the use of button "ZPenable" (Switch-2, Sheet 5), which is on the front panel.
For improving reliability of programme operation and for avoiding false activations, caused by external factors (for example noises), as well as for forming final signals there have been used triggers JK (Sheet 7, Fig. 2). As clock signals there has been used dual clock signal CLK_ 2(Sheet 7, Fig. 1).
Technical measurements (analysis) show that activation of signals occur in 40us-80us, and blocking of Pulse Gate and Rectifier in about 100us-180us (switching time optocouplers GN32).

Hardware Description

All Interlock signals generated in different devices are connected to the experimental board through respective stecker (Sheet 3). These signals come from:

- Chopper to X 32 _A (3M40)
- Electronics to X 21 _A (3M40)
- External devices to X03 _A (3M16)

There is a possibility of manual (mechanical) activation of any of these signals with the use of stecker JP03-A (Sheet 3).
For determining the status of these signals they are connected through resistor (1KΩ) to the voltage of +5V (logical value HIGH). With the proper operation all relays of devices are connected to GND, and these signals get value LOW (generally, LOW-O'K, HIGH – not O'K).
During switching signals from devices to board they can be affected by different external factors (for example, close wires of high voltage). For this reason before passing them to the software (Altera Chips) they go through IC01-A and IC02-A (Hex Schmitt Triggers, series of MC14584), Sheet 4. After that status signals, already "cleared" from undesirable noises and inverted go on software as input status signals.
Status of all input signals is indicated with LED on the front panel.
Output signals coming from software are also indicated on the front panel. These are:

- LED-ZPein (Position of Puls Gate)
- LED-Turn Off PS (Position of Power supply)
- LED-Beam Inhibit (Position of Damp)

For control of operational voltage +24V on the front panel there is a signal lamp "LED-24V OK", which indicates voltage value (Sheet 5 and Sheet 6).

Power tests

To feed the PS Test Stand DC Power Supply has been built . It is constructed as separate unit and comprises the following components:

- Autotransformer ATR for regulation of voltage with the commutation apparatus Q1.1 and K1.1.
- Transformer 400/60V for galvanic separation and impedance matching
- 6 pulse diode rectifier (D1-D6)
- LC smoothing filter with parameters: L = 1mH, C = 14.5 mF

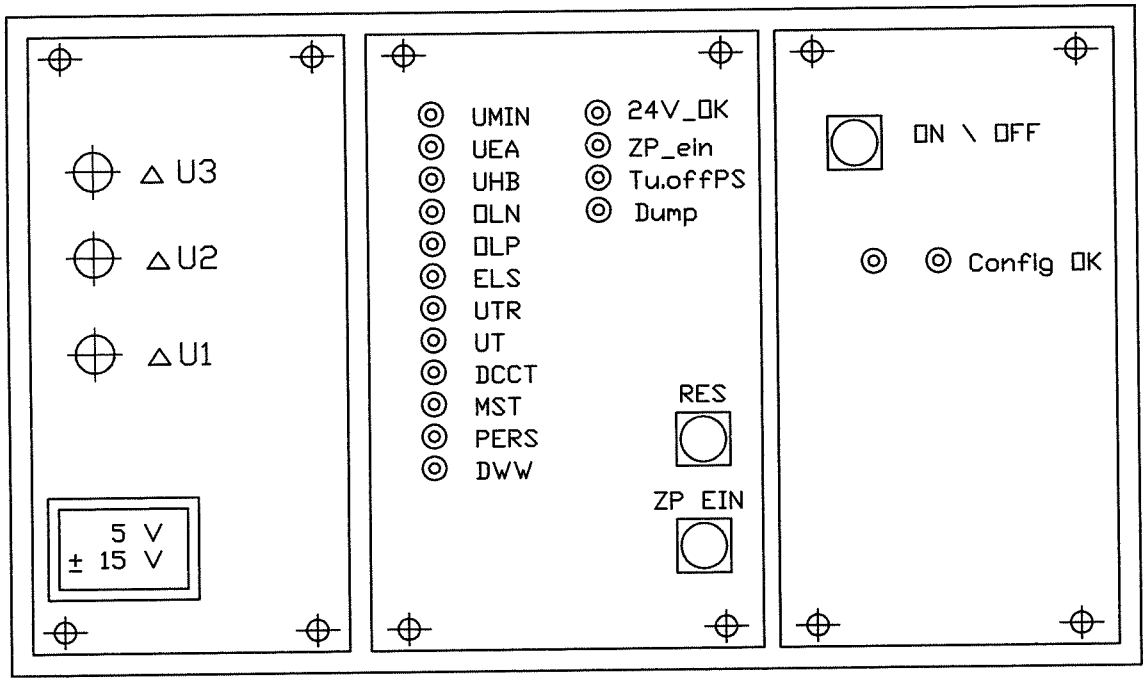
A primary DC voltage is being switched by a Pulse Width Modulation (PWM) with 16 kHz frequency. The power supply has been tested for up to 60A of the load current at 80V.

Testing of all the Programme modules including the Main Interlock Programme, Reset Programme, and Programme for external devices and Test of lamps shows satisfactory results.

The personal involved in the Project are:

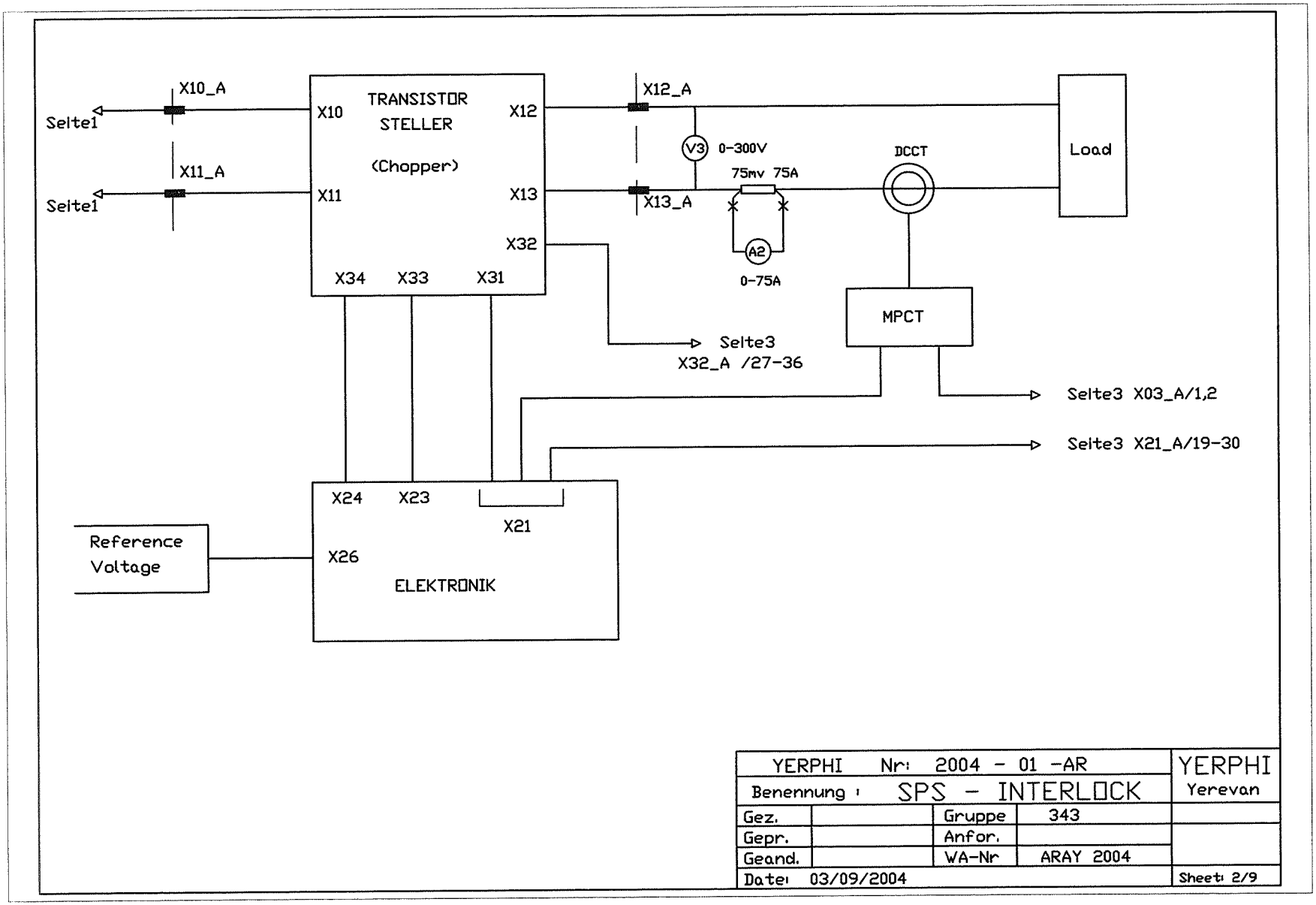
Dr. Hamlet Martirosyan, head of laboratory
Davtyan Kamo, engineer
Khachatryan Rubik, engineer
Mkrtchyan Araik, engineer
Ayrapetyan Vardan, technician
Khosrovyan Stanislava, worker

Coordinators:
J-P.Jensen, N.Heidbrook, H-J.Eckoldt, (DESY)
H.Martirosyan, V.Nikoghosyan , (YerPhI)



Power Supply ±15v 5v	Inerlock Board	ALTERA Board

YERPHI Nr: 2004 - 01 -AR				YERPHI Yerevan
Benennung : SPS - INTERLOCK				
Gez.		Gruppe	343	
Gepr.		Anfor.		
Geand.		WA-Nr	ARAY 2004	
Date: 03/09/2004				Sheet: 1/9


X10_A
Seite1
X11_A
Seite1
X10
TRANSISTOR
STELLER
(Chopper)
X11
X12
X13
X32
X34
X33
X31
X12_A
V3
0-300V
X13_A
75mv 75A
DCCT
A2
0-75A
Load
MPCT
Seite3
X32_A /27-36
Seite3 X03_A/1,2
Seite3 X21_A/19-30
X24
X23
X21
Reference
Voltage
X26
ELEKTRONIK
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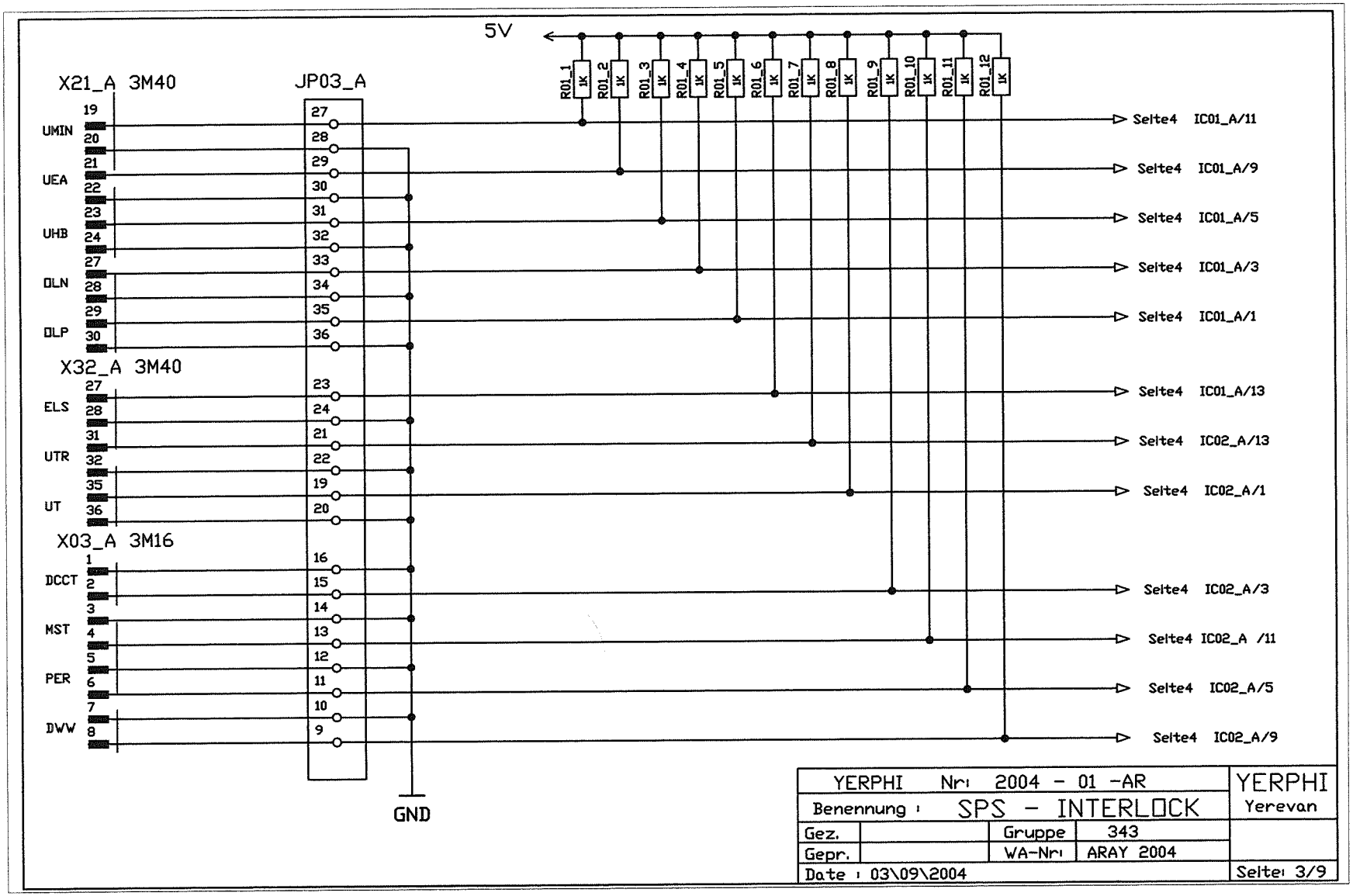
5V
X21_A 3M40
JP03_A
UMIN
UEA
UHB
DLN
DLP
X32_A 3M40
ELS
UTR
UT
X03_A 3M16
DCCT
MST
PER
DWW
GND
R01_1 1K
R01_2 1K
R01_3 1K
R01_4 1K
R01_5 1K
R01_6 1K
R01_7 1K
R01_8 1K
R01_9 1K
R01_10 1K
R01_11 1K
R01_12 1K
Seite4 IC01_A/11
Seite4 IC01_A/9
Seite4 IC01_A/5
Seite4 IC01_A/3
Seite4 IC01_A/1
Seite4 IC01_A/13
Seite4 IC02_A/13
Seite4 IC02_A/1
Seite4 IC02_A/3
Seite4 IC02_A /11
Seite4 IC02_A/5
Seite4 IC02_A/9
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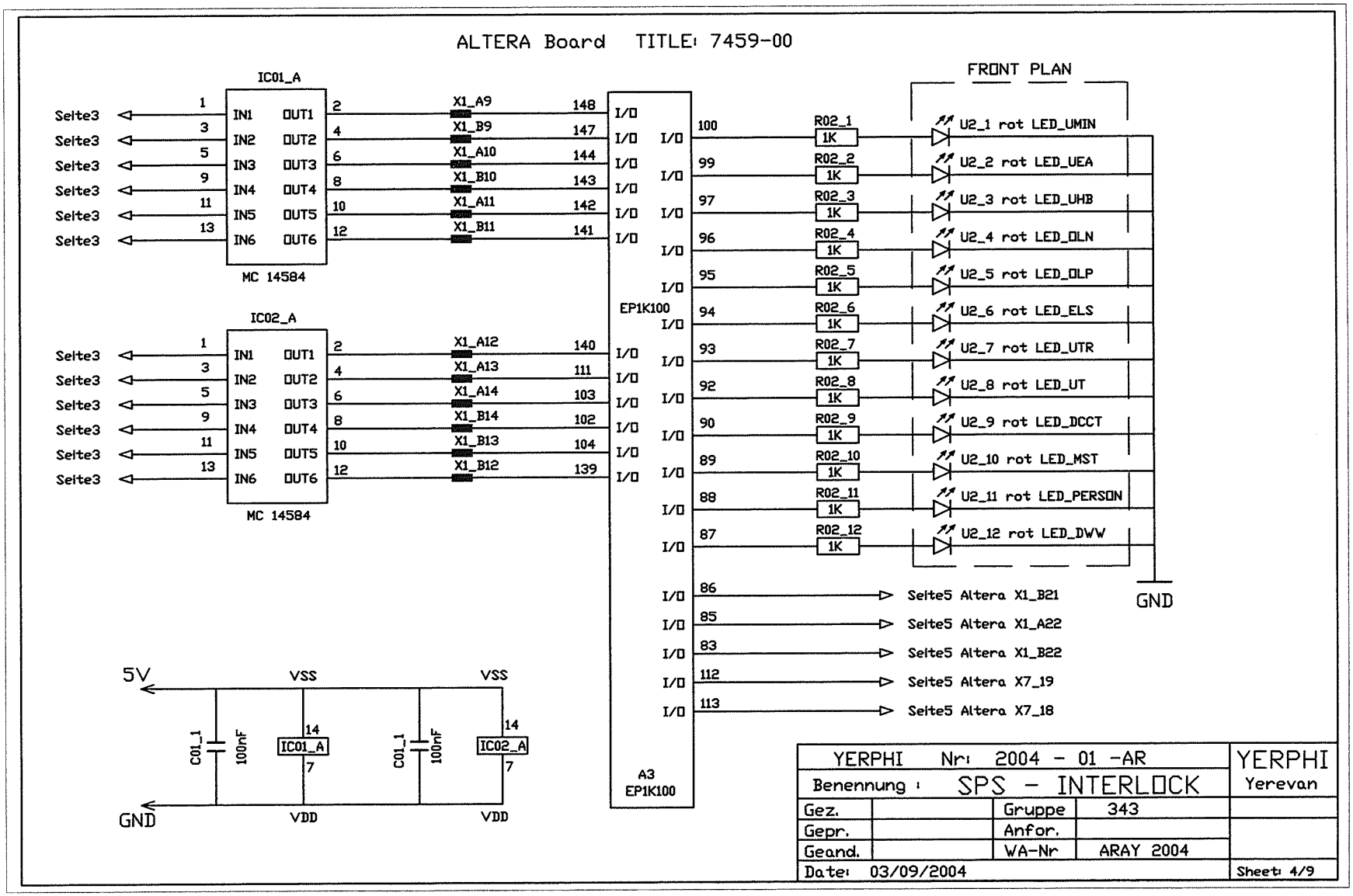
ALTERA Board TITLE: 7459-00
IC01_A
IC02_A
MC 14584
MC 14584
Seite3
IN1
IN2
IN3
IN4
IN5
IN6
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
X1_A9
X1_B9
X1_A10
X1_B10
X1_A11
X1_B11
X1_A12
X1_A13
X1_A14
X1_B14
X1_B13
X1_B12
EP1K100
A3
EP1K100
I/O
FRONT PLAN
R02_1
R02_2
R02_3
R02_4
R02_5
R02_6
R02_7
R02_8
R02_9
R02_10
R02_11
R02_12
1K
U2_1 rot LED_UMIN
U2_2 rot LED_UEA
U2_3 rot LED_UHB
U2_4 rot LED_OLN
U2_5 rot LED_OLP
U2_6 rot LED_ELS
U2_7 rot LED_UTR
U2_8 rot LED_UT
U2_9 rot LED_DCCT
U2_10 rot LED_MST
U2_11 rot LED_PERSON
U2_12 rot LED_DWW
GND
Seite5 Altera X1_B21
Seite5 Altera X1_A22
Seite5 Altera X1_B22
Seite5 Altera X7_19
Seite5 Altera X7_18
5V
VSS
VSS
C01_1
100nF
C01_1
100nF
IC01_A
IC02_A
GND
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VDD
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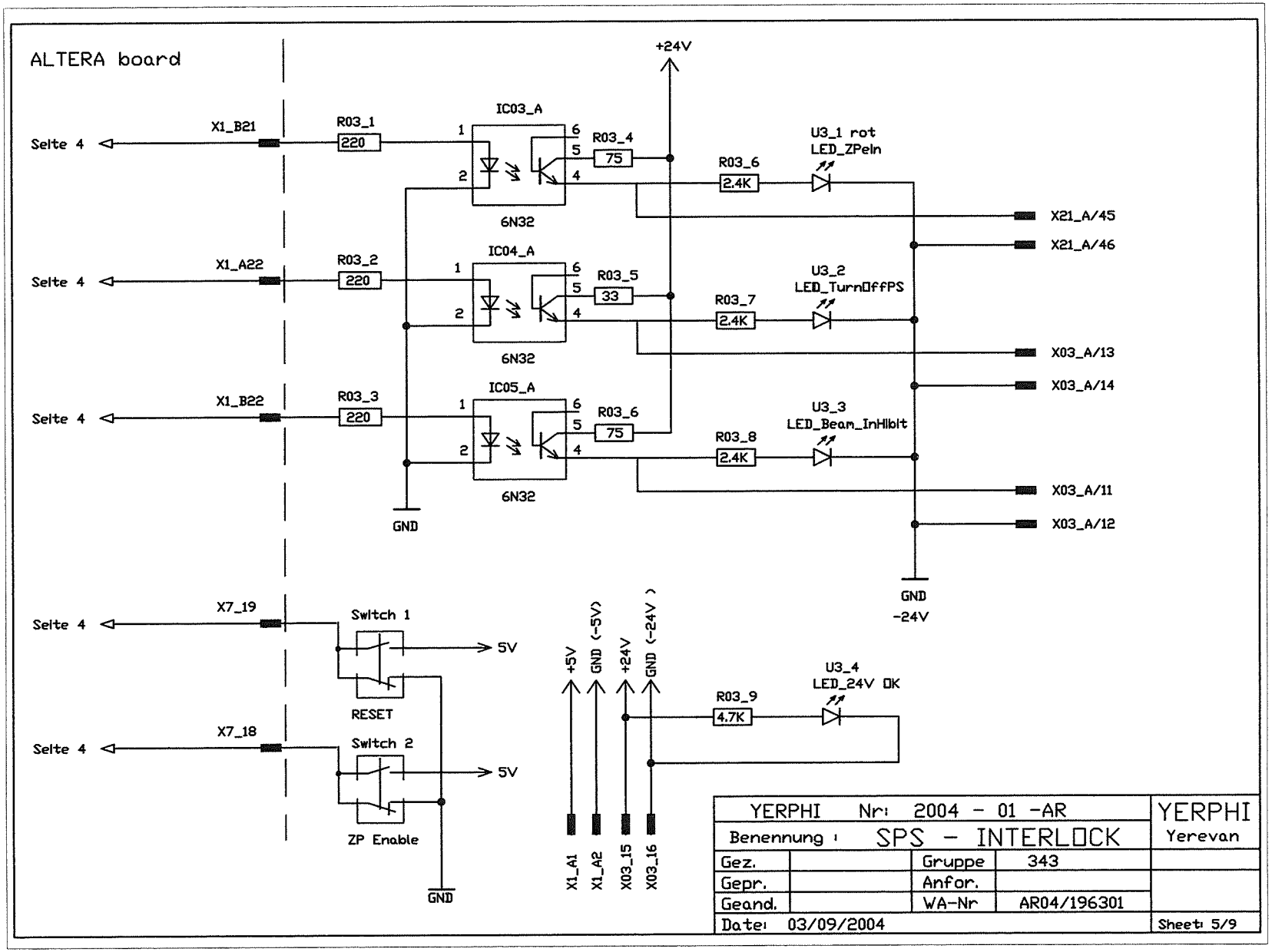
ALTERA board
+24V
Seite 4
X1_B21
R03_1
220
IC03_A
1
2
6
5
4
R03_4
75
R03_6
2.4K
U3_1 rot
LED_ZPeln
6N32
X21_A/45
X21_A/46
Seite 4
X1_A22
R03_2
220
IC04_A
R03_5
33
R03_7
2.4K
U3_2
LED_TurnOffPS
6N32
X03_A/13
X03_A/14
Seite 4
X1_B22
R03_3
220
IC05_A
R03_6
75
R03_8
2.4K
U3_3
LED_Beam_InHibit
6N32
X03_A/11
X03_A/12
GND
GND
-24V
Seite 4
X7_19
Switch 1
5V
RESET
Seite 4
X7_18
Switch 2
5V
ZP Enable
GND
+5V
GND (-5V)
+24V
GND (-24V)
R03_9
4.7K
U3_4
LED_24V OK
X1_A1
X1_A2
X03_15
X03_16
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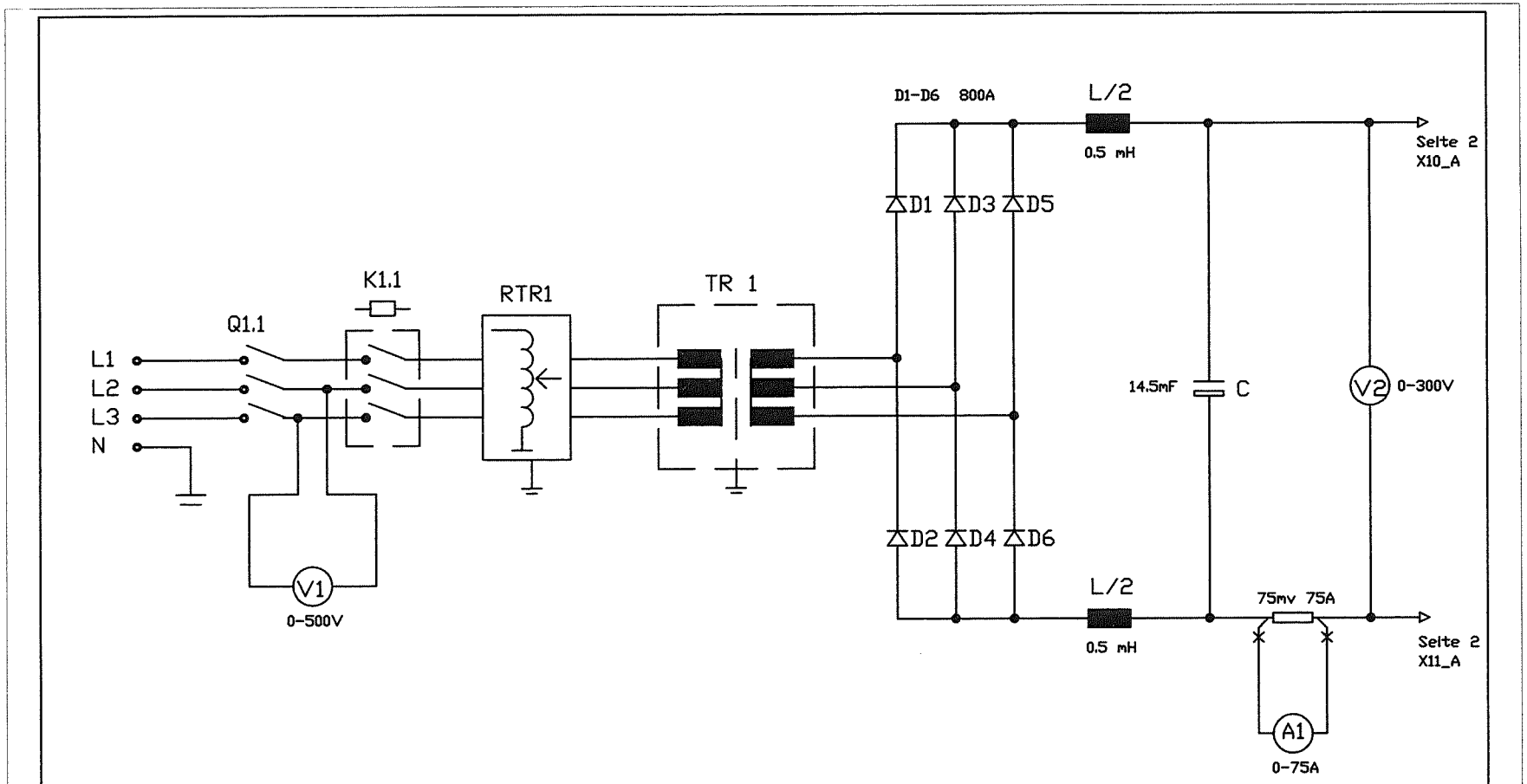

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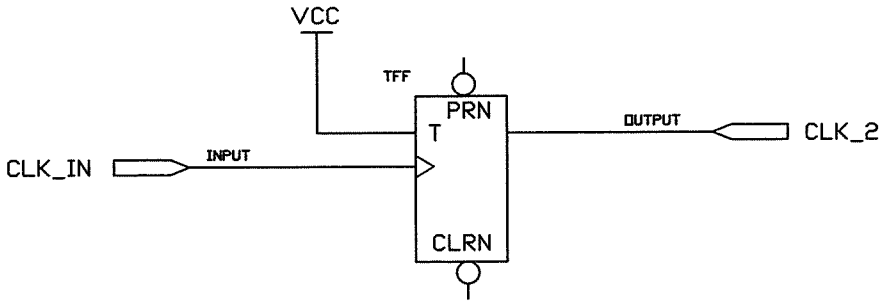

Fig. 1

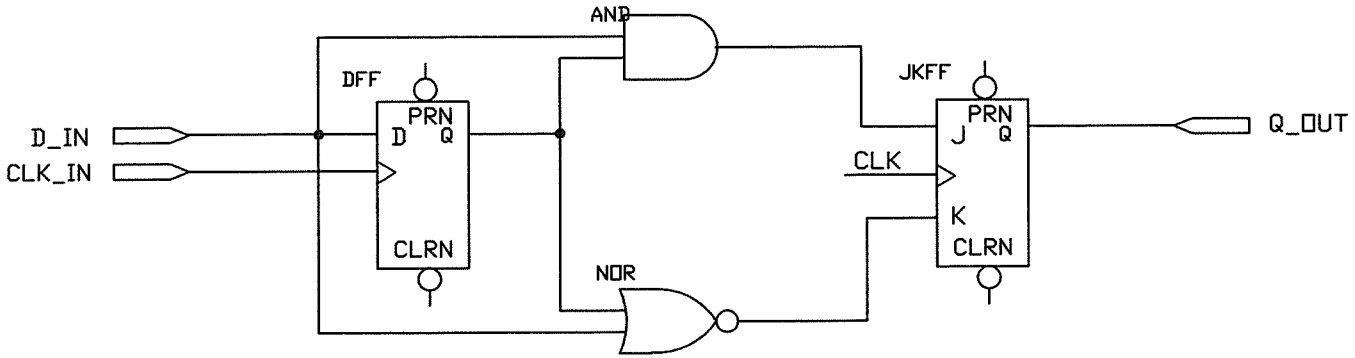

Fig. 2

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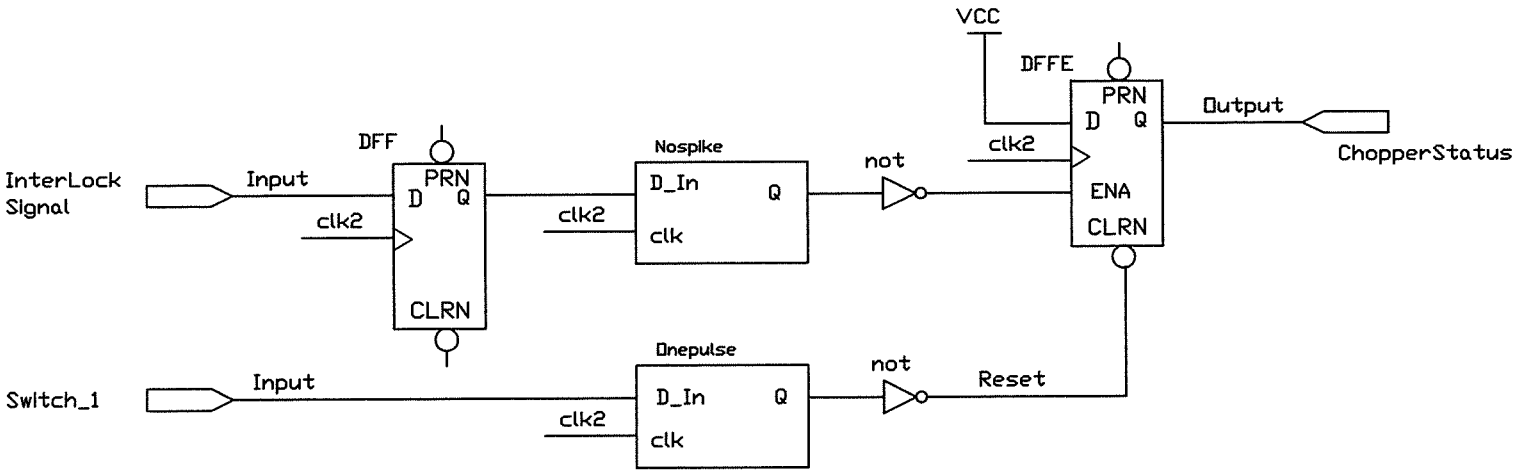

Fig. 1

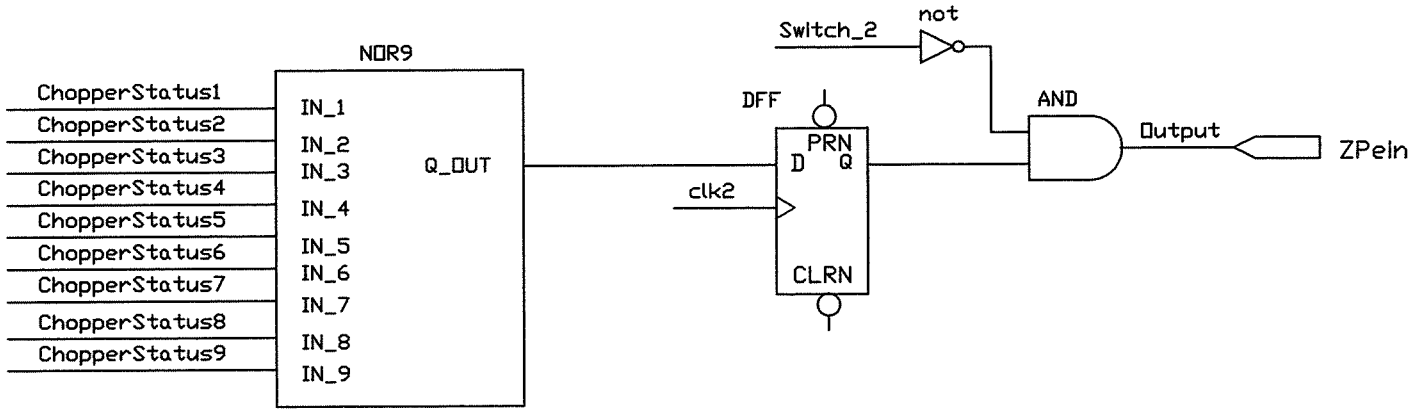

Fig. 2

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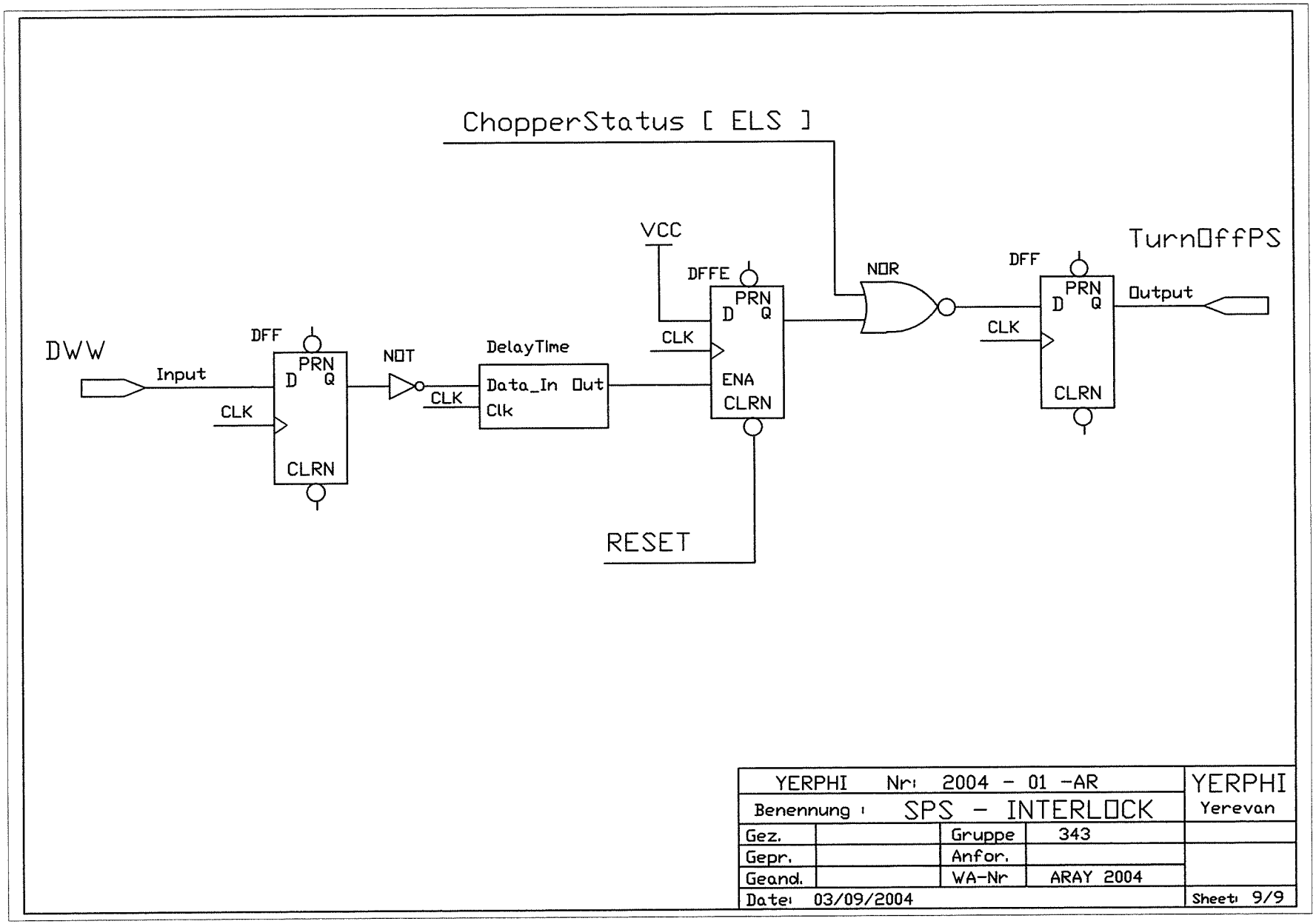

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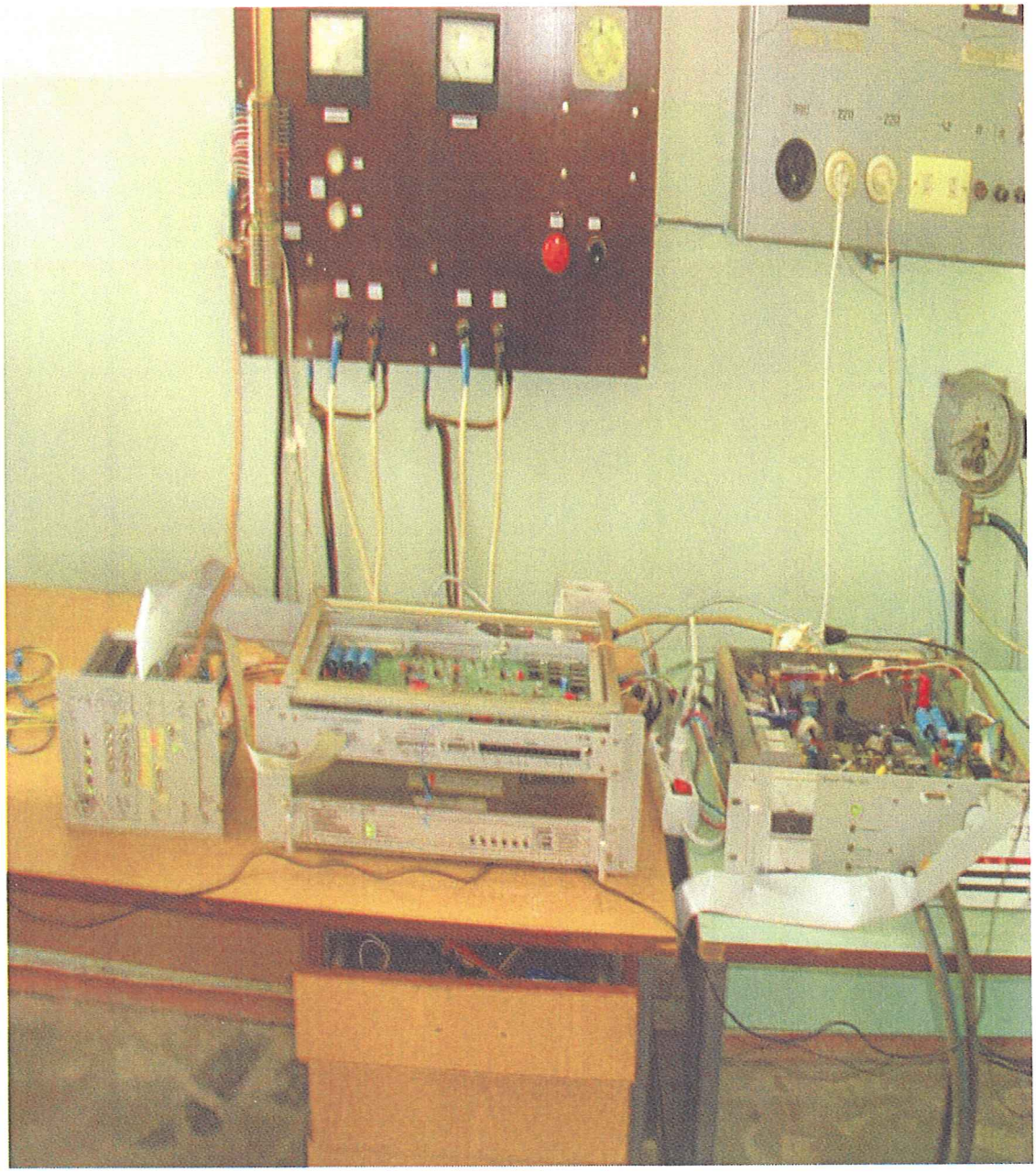
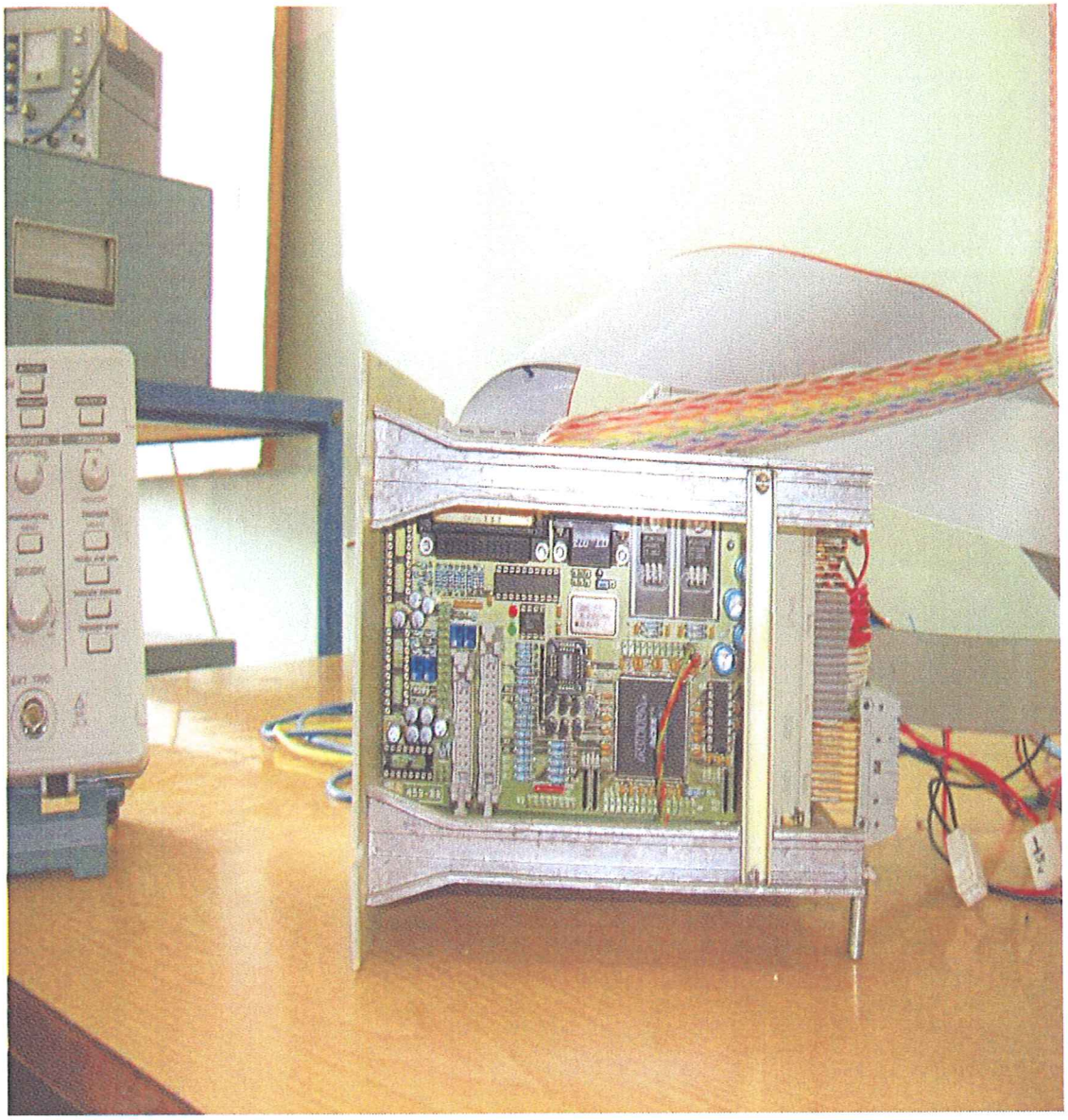
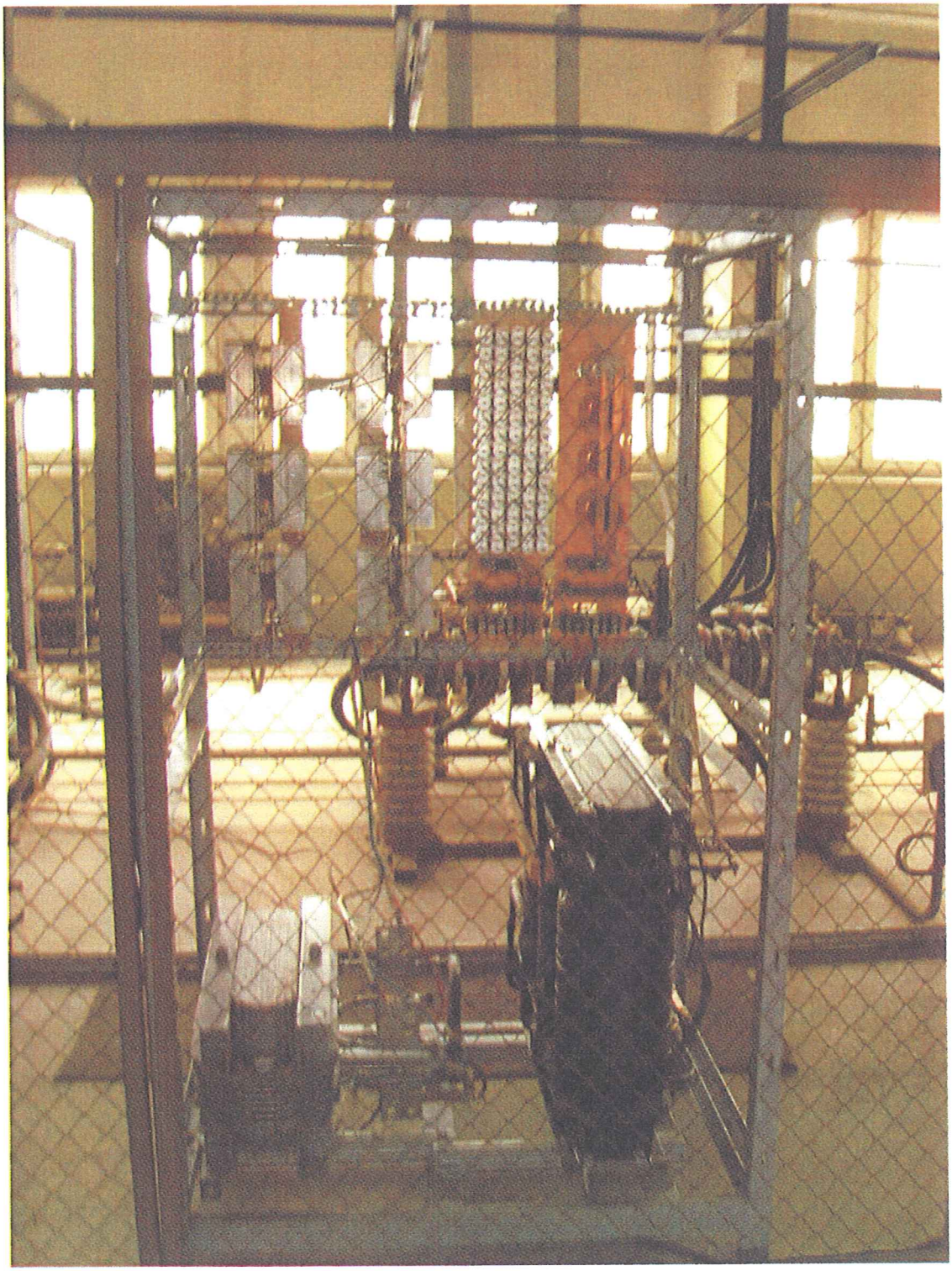


Test Stand

Part of Test Stand



Digital Control Board for INTERLOCK



DC Power Supply