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Results from End-of-Substructure card production for the ATLAS ITk Strip upgrade using both the lpGBT-v1 and -v2 ASIC

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Abstract: The tracking system of the ATLAS experiment will be upgraded for the upcoming High-Luminosity Upgrade of the LHC (HL-LHC). The main building blocks of the new strip tracker are silicon-strip modules that consist of a sensor and hybrid PCB's. The modules are mounted on rigid carbon-fibre substructures, the so-called staves (petals) in the barrel (end-cap) regions, that provide common services to the modules. At the end of each stave or petal side, a so-called End-of-Substructure (EoS) card facilitates the transfer of data, power, and control signals between the modules and the off-detector systems. The EoS connects up to 28 data lines, each with 640 Mb/s, from the modules to one or two lpGBT chips that provide data serialization and use a 10 Gb/s versatile optical link (VL+) to transmit signals to the off-detector systems. The lpGBT also recovers the LHC clock on the downlink and generates clock and control signals for the modules. To meet the tight integration requirements in the detector, fourteen different EoS card designs are necessary. The power to the EoS is provided by a dedicated dual-stage DC-DC package providing 2.5 and 1.26 V to the EoS cards. A first production of almost 2000 EoS cards has been stopped due to the errors found in the lpGBT-v1 ASIC, but all

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accompanying DC-DC converters have been produced. We report on the production experience including detailed QC statistics and design validation (QA) results for the EoS itself with the lpGBT-v1 ASIC and how the two lpGBT issues were identified and how many EoS boards were affected by each. With the lpGBT-v2 ASIC now in hand, we report first QC results with the second production iteration.

KEYWORDS: Electronic detector readout concepts (solid-state); Front-end electronics for detector readout; Particle tracking detectors (Solid-state detectors); Si microstrip and pad detectors

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1 The inner tracker (ITk) for the high-luminosity upgrade of the ATLAS experiment

The ATLAS Experiment [1] at the LHC [2, 3] will be upgraded for the high-luminosity period. The inner tracker, see figure 1, will be replaced by an all-silicon tracker, called the 'ITk'. The innermost part consists of a silicon-pixel detector, described in more detail in [4]. The silicon-strip tracker consists of a central barrel region with four cylindrical layers and two end-cap-regions, each with six disks. These layers will be composed out of substructures, for the barrel 1.4 m long 'staves', oriented parallel to its axis, and for the end-caps radially oriented 0.6 m long 'petals'. For the barrel, one stave points along the cylinder axis away from the central plane to the positive side and another to the negative. The readout electronics is connected at both ends of the barrel and at the outer radius of the end-caps. More details of the detector design can be found in the ATLAS-ITk Technical Design Report [5].

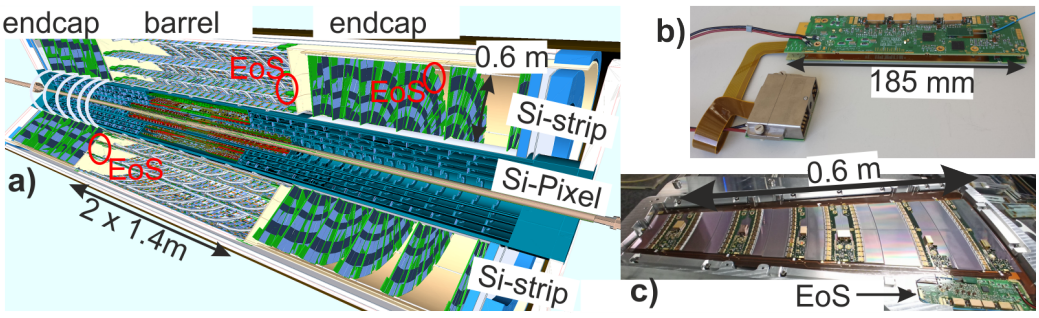

Figure 1. (a) The layout of the inner tracker for the ATLAS experiment, which is in construction for the high-luminosity LHC data taking. Reproduced from [5]. CC BY 4.0. (b) a pair of EoS card as assemble for one substructure (stave), (c) a substructure (petal) with assembled sensors, hybrids and an EoS card on a carbon-fibre core. Reproduced with permission from [6]. CC BY-NC-ND 4.0.

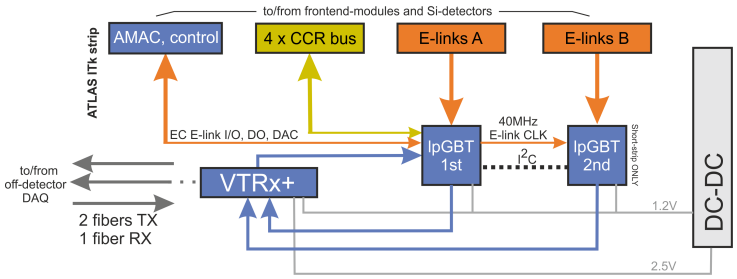

Figure 2. Block-diagram of an EoS card using the ASICs designed by CERN-EP-ESE. Reproduced from [14]. The Author(s). CC BY 4.0.

2 Electronics at the end of the substructures: EoS cards

At the end of each substructure, the so-called End-of-Substructure (EoS) cards are mounted. These printed circuit boards (PCB) interface the front-end electronics with the off-detector system, see figure 2. The EoS communicates with the off-detector system via the VTRX+-module and optical fibres [7]. The optical receiver provides 2.5 Gb/s for the RX-link (to the EoS) and 10 Gb/s for the TX-links (from the EoS). The power and some critical signals are using electrical cables. The lpGBT-ASICs [8] convert the RX-link to signals for the front-end modules and multiplex the 14 or 28 incoming data-streams (640 Mb/s), E-links-A/B, from the front-end modules to one or two TX-links. With the connection to the front-end modules the following is distributed:

- Low-voltage (10–12 V, <10 A),
- High voltage for biasing silicon sensors (<550 V, <15 mA),
- Three or four CCR-buses for LHC-synchronized Clocks, Control and Reject signals (160 Mb/s),
- Slow signals to and from the AMACs [10] for configuring and monitoring.

The mechanical integration of the EoS cards to the substructures, see figure 1 and for details [11], is performed by gluing a pair of EoS cards to both sides of a carbon-fibre structure, which supports also the sensors with their electronics. The electrical interface to the off-detector electronics is a bulky connector, which is screwed to the overall support structure of the ITk. Because the connector positions need to follow mechanical constraints for the overall integration, connection between the connector and the active part requires a flex-lead as integrated part of the PCB. Its geometry and by that the design needed to be adapted for different locations within ITk. For more details of the design see [12].

In total 2000 cards will be produced. Since these are divided into 14 different flavours, the number of cards per individual flavour can be as low as 14. This complicates the production and the tests for quality-control, because only very low statistics can be accumulated on the individual flavour issues. Just for the common behaviour the statistics is sufficient to detect low-rate problems.

Three different versions of the lpGBT-ASIC have been used: v0, v1 and v2. The early version — v0 — was used for validating the design in the early phase of the project. The v1 version was used in production until serious faults were discovered, which are described in section 4 and 5. A new version, v2, addressing the faults discovered in v1, was delivered by the design-team (CERN-EP-ESE) [9] and the production of the EoS cards was restarted. To date, 1031 cards with the lpGBT-v1 were populated and 300 cards were tested before the faults could be reliably identified. 200 cards with the lpGBT-v2 have been tested at the time of writing.

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3 Quality Control (QC) during the workflow

During production, the whole workflow is accompanied by test of the involved components. Ensuring quality and minimizing later faults are essential, because the EoS cards are single point of failures for a complete side of a substructure. The QC starts with the production of the PCBs and ends with the packaging for sending the EoS-modules for integration into the substructures.

- The bare printed circuit board (PCB) production was performed at an external company. There QC-checks cover the etching per layer, the geometry, the dimensions, the drilling, the metallization (see figure 3), the impedances and the connectivity matrix.
- A custom test coupon, specially designed for usage by the EoS-QC team, is part of each EoS-production-panel. It is populated with the same process and machine as later the EoS cards themselves. QC-checks allow to verify the impedances, the resistance of 1 m-long traces on each layer and the ability to solder same pitch-Ball-Grid-Areas (BGA) (0.5 mm) and to bond onto the Cu-Ni-Au-surfaces (ENIG) of the pads.
- After performing the SMD-soldering, every component and solder-joint are checked with an automated optical inspection. While positioning the BGA the presence of each solder ball is checked optically.
- The boards are sent out to an external institute for an X-ray control of the BGA soldering, since that is hidden and no more visible below the chip itself (figure 3).
- The through-hole soldering of the electrical connector to the off-detector system is performed afterwards.
- The final QC-tests for functionality, mechanical integrity and dimensions are then taking place. Using a fine-pitch (0.7 mm) needle prober each input or output can be connected and by that the full functionality for digital and analogue performance can be checked. Another test allows to thermal cycle the PCB's down to -35 °C and to 25 °C and perform basic function test over the entire temperature range. For the high voltage the isolation is checked up to (1.1 kV) twice the maximum operation voltage with TΩ-measurements. All tests monitor the voltage, current and temperature behaviour. Dedicated emphasis is given to the high speed data lines RX, see section 5, and TX. For the TX special firmware allows recording the eye diagrams without a company-specific protocol and during normal operation.
- Just before packaging final optical checks are performed to exclude mechanical damages that might happen during handling for the QC.

In figure 3 examples of the QC-tests are demonstrated, which are selected from two different production steps. For the in-house QC, the RX-checks are described in section 5. Details to the test and the equipment are described in [13] and [14].

4 Identified faults in the lpGBT-v1 and solved for the version v2

Statistics from 300 EoS cards with lpGBT-v1 were accumulated. Two error modes inside the lpGBT were identified and were discussed with the ASIC-design team [8, 9]. At start-up, the clock-tree

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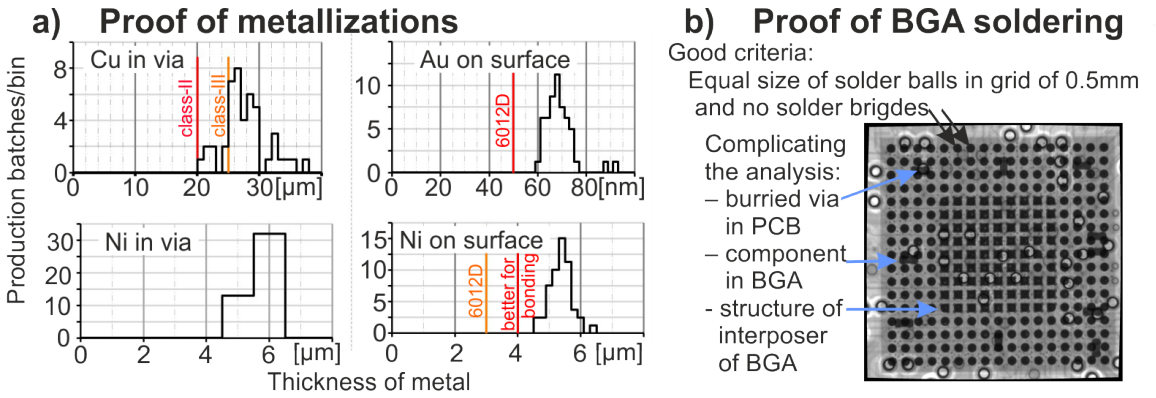

Figure 3. Examples of the QC-tests performed at the different stages of the production: (a) metallization at the PCB-manufacturer compared to the requirements from IPC 6012D and our own requirement as compromise to the fine pitch BGA and experience for bonding, (b) X-ray of the BGA-area demonstrating that the amount of tin is good for contacts, but avoids short-circuits.

lock-out feature had a 2.3 % probability of disabling at least one lpGBT on the EoS without any possibility to reset the chip. The behaviour of any individual chip is expected to change over time: fully functional chips may turn faulty and vice versa.

The per-default enabled attenuator for the RX-signal [8] caused a baseline shift in the receiver (figure 4). The logic state of the bits made the RX-link inoperable for about 2.6 % of the chips, and since on a system-level the attenuator setting can be modified by the RX-link only, the situation ends in a dead loop. To address both faults, the ASIC-designers [9] modified metal layers of the ASIC and processed with a fast reproduction, allowing lpGBT-v2 delivery with shorter delay than initially feared.

5 The analysis of the received RX-signal from off-detector

The lpGBT-ASIC provides the option to record the eye diagram for the receiver-link RX at 2.5 Gb/s. An individual pixel of the diagram is selected by setting a delay and a threshold. At these settings the logic state is identified as '0' or '1'. For a stream of $N_{\text{Stream}} = 2^{17}$ bits the identified transitions from '0' to '1' are counted. In the open eye, the yellow part in figure 4, each transmitted bit-sequence '01' increments the counter by one. For the pixels in the top triangle between the edges (green) a sequence '011' (bottom '001') is required. For a fully random bit-stream with a 50 % chance to get a state '0', the mean of the counters and the widths of the distributions (Root-Mean-Square) can be calculated:

$$\text{Mean}_{\text{Open}} = N_{\text{Stream}}/4 \qquad \text{Width}_{\text{open}} = \sqrt{N_{\text{Stream}} \cdot 1/16}$$

$$\text{Mean}_{\text{Triangle}} = N_{\text{Stream}}/8 \qquad \text{Width}_{\text{Triangle}} = \sqrt{N_{\text{Stream}} \cdot 3/64}$$

The measured widths agree very well with the expectation and the measured means are shifted only very slightly: for the open eye by 13 from 2^{15} expected counts and for the triangles by 275 from 2^{14}. The reason for the shifts is not identified. They may be a consequence of the non-perfect randomness of the balanced bitstream. Between these two peaks the histogram is defined by the smooth transition from open eye to uncertain identification and the continuous population is expected. The tail towards zero reflects the transition region to too extreme thresholds, for which either the '0'- or the '1'-state is no longer reachable. By that the eye diagram is well understood. The criterion for defining functional

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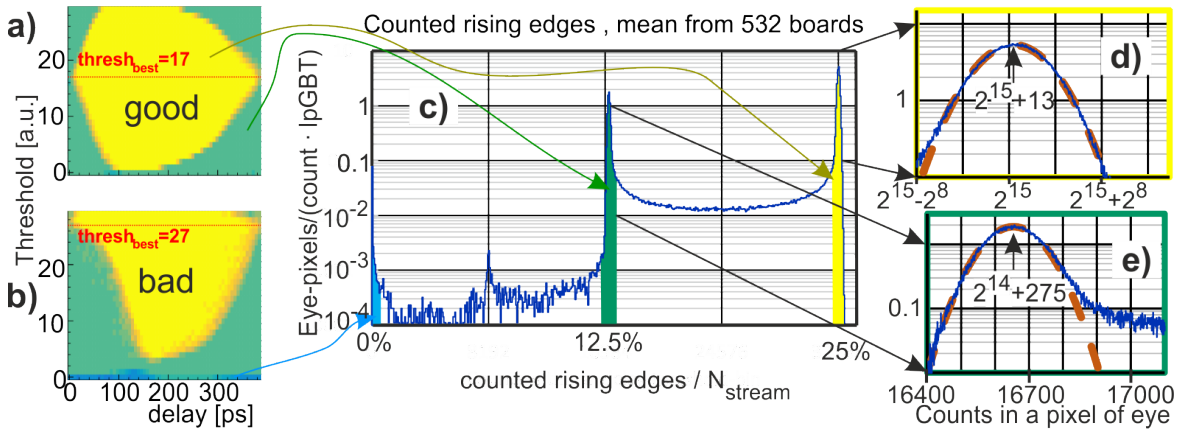

Figure 4. Analysis of the eye diagram for RX: (a) a good eye diagram, (b) a bad eye diagram with offset in the receiver, (c) Statistics of pixels with given count over the whole eye diagram summed over all tested cards with lpGBT-v1, (d) zoom into the peak for the open eye (yellow) region, (e) zoom into the region between the slopes (green). For (d) and (e) the curves are Gaussian with the width as expected from stochastics, but shifted to the measured mean.

and faulty EoS cards does not benefit from these details, but they increase the overall confidence in the eye diagram. The position of the threshold, which has the highest sum of counts in its row, is already a sufficient criterion to define a card as functional or faulty [14]. This offset reflects the cause on transistor-level and is not expected to change over time or with uncontrollable operation parameters [9].

6 The statistics of the faults for EoS cards with lpGBT-v1 and lpGBT-v2

In the QC-tests on the board with lpGBT-v1, 0.8 % of the EoS cards failed due to the disabled clock-tree and 0.7 % due to the enabled attenuator in the RX-receiver. For the new production with lpGBT-v2 none of 200 boards showed these errors. While for the first production 1.6 % of the cards show faults on the custom-test-coupons or by handling, this rate is also reduced to 1 % with the second production, which is compatible within errors with the previous production run.

7 Outlook

The lpGBT-v2 solves the issues identified within the lpGBT-v1, however most of the EoS production has to be redone. To maintain the overall schedule of the ATLAS upgrade, selected existing EoS cards with the lpGBT-v1 will be used in the beginning of the production. The selection-criteria are no identified start-up error in all the QC-cycles and a centred baseline for the RX-signal, which is expected to be stable over time. In doing so, an acceptable performance is expected and the construction schedule can be met.

Acknowledgments

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