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PETRA-IV FOFB SYSTEM INTEGRATION TEST SETUP

B. Dursun*, S. H. Mirza, S. Pfeiffer, A. Eichler, H. Schlarb, H. T. Duhme, G. Kube
Deutsches Elektronen-Synchrotron DESY, Hamburg, Germany

Abstract

The PETRA-IV Fast Orbit Feedback (FOFB) system will be a large-scale Multi-Input Multi-Output (MIMO) control system, utilizing 790 Beam Position Monitors (BPM) and 560 Fast Corrector Magnets (FCM) to maintain the desired orbit trajectory. Data acquisition and distribution will be managed across 16 supply areas and connected via an extended star network topology. This contribution focuses on system integration test setups while describing the Model-Based Design (MBD) methodologies that are being used for developing, verifying, and commissioning the complete system step by step. Integration of the components of such a large system must be systematic so that potential issues can be isolated and fixed efficiently. The setups will also be used for the characterization of sensors, actuators, and transmission lines. Subsystem identification is of utmost importance for a comprehensive understanding of the system dynamics, which will guide the design of appropriate filters and control strategies to ensure optimal orbit stabilization performance. The analysis will also precisely assess the overall system latency, which is critical for feedback bandwidth and stability.

INTRODUCTION

The PETRA-IV project at DESY aims to upgrade the present PETRA-III synchrotron into a fourth-generation, ultra-low emittance source operating at 6 GeV. The target emittance is 20 pm·rad horizontally and 4 pm·rad vertically, which translates into significantly smaller beam sizes, approximately 7 µm horizontally and 3 µm vertically at the insertion device (ID) source points. The FOFB system is a crucial component for rejecting disturbances up to 1 kHz, thereby ensuring the required stability of 10% of the beam size [1]. This represents a significant improvement over third-generation light sources, where disturbance rejection bandwidths were typically limited to a few hundred Hertz.

This work focuses on the methodology being used in the development process of the FOFB system. It describes the model-based workflow, which utilizes the Model-In-the-Loop (MIL), Software-In-the-Loop (SIL), and Hardware-In-the-Loop (HIL) simulations throughout the design, implementation, and verification stages. The paper also details the setups being designed for integration tests and system identification. In addition to scope-specific real-time emulators, such as the beam emulation used for BPM system identification and BPM-FOFB integration, the complete system will feature an operational mode to run a real-time plant emulator for final verification before commissioning tests.

PETRA-IV FOFB SYSTEM OVERVIEW

The FOFB system is designed in an extended star topology, featuring one global node (GOC - Global Orbit Controller) and 15 local nodes (LOC - Local Orbit Controller) distributed across supply areas (Fig. 1). Each LOC is the center of regional sensor and actuator stars. Feedback from BPM processors (BPM_P) will be aggregated through sensor hubs (BPM_H), and the control action will be distributed to the FCM drivers (FCM_D) through actuator hubs (FCM_H).

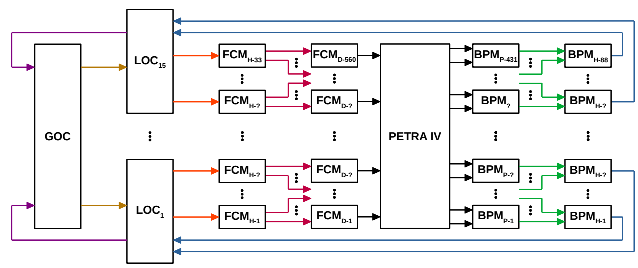

Figure 1: PETRA-IV FOFB block diagram.

The complete signal chain is planned to be realized in the MicroTCA.4 form factor excluding FCM_D. Fig. 2 illustrates the hardware layout at each supply space. The GOC will be located at Supply Space 1, with direct optical links to all LOCs. This standardized approach enhances modularity and maintainability while supporting the high-speed data processing required for the FOFB system.

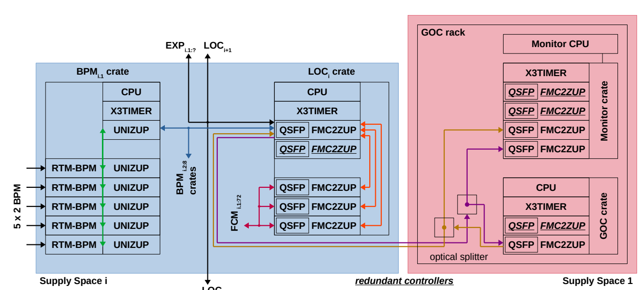

Figure 2: Hardware layout in the MicroTCA.4 form factor.

The rate of the closed-loop control operation will be 130 kHz, equal to the revolution frequency. Data propagation is optimized to minimize the overall latency. The total loop latency is estimated to be a maximum of 80 µs, which includes delays from sensors, actuators, communication links, and the controller. This latency budget is critical for achieving the desired feedback bandwidth and stability.

Data propagation in the processing chain is visualized in Fig. 3. The communication links from BPM_P to BPM_H, and from LOC to FCM_D are latency-optimized, while other links

* burak.dursun@desy.de

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are throughput-optimized. During BPM signal processing, the data will be tagged with a revolution identifier, allowing for temporal alignment of the data to compensate for the large path length differences between the GOC and the LOCs. Similarly, the FOFB control action will be tagged for each FCM_D with the same revolution identifier and applied in coordination. In addition to the fundamental and unidirectional information for the control loop, the payload of transactions will be extended bidirectionally for exception handling.

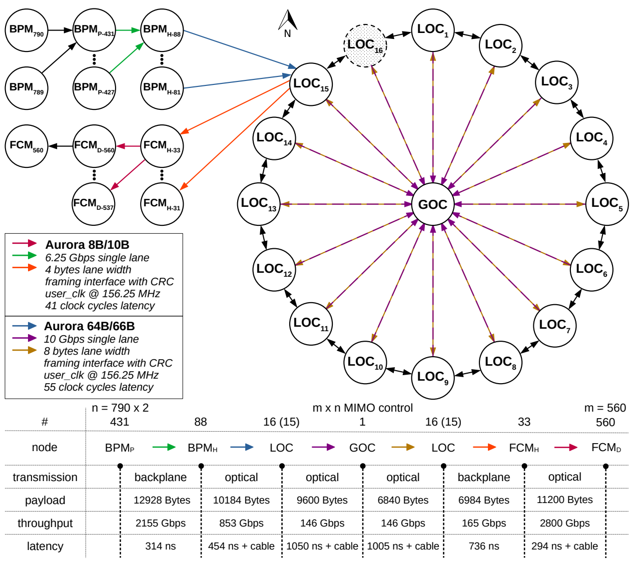

Figure 3: Network topology and link configuration.

MODEL-BASED DESIGN AND FIRMWARE DEVELOPMENT

The performance of the FOFB system is determined by the beam stability requirements, which in turn follow from the lattice design provided by the Accelerator Physics Department. Therefore, the development of the FOFB controller began with simulations based on lattice models and is complemented by empirical models of FOFB components and disturbance sources [2]. These empirical models are refined through beam position spectra and electronics noise measurements at PETRA-III using the PETRA-IV BPM system, ground vibration studies supported by Distributed Acoustic Sensing (DAS) technology, and domain-specific simulations for cables, corrector magnets, and the beam pipe in the actuator chain. The simulations that utilize both the controller and the plant model completely within a high-level software environment are defined as MIL. As the core of the development process, this phase specifies the system that all subsequent steps will be dedicated to accurately realizing (Fig. 4).

The following development steps include implementation and soft-verification. During the implementation phase, the controller model serves as the requirements specification, and the algorithm is optimized in accordance with the

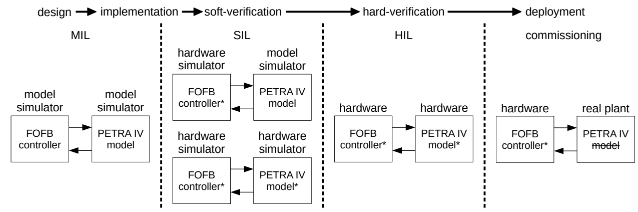

Figure 4: Model-based development flow.

target Field Programmable Gate Array (FPGA) architecture. The assessment of the optimization process is critical, as the intended behavior may diverge if it is not tracked against the model. The infrastructure being used for this soft-verification process is defined as SIL simulations, which utilizes the plant model in high-level software while the implementation of the controller is running on a hardware simulator (Fig. 4). More specifically, it is a co-simulation environment that integrates Python-based models with Hardware Description Language (HDL) simulators. The soft-verification stage can lead to iterations on implementation, and even design updates may be required.

Prior to the final commissioning process, the complete system is planned to be verified via HIL simulations. This phase is defined as hard-verification, which utilizes real-time plant model emulation against the production-ready FOFB system. Real-time emulation of PETRA-IV is as challenging as the controller design and implementation. Hence, this process also requires SIL simulations for soft-verification before the physical integration of the system. HIL simulations will then be used to verify the success of this integration (Fig. 4).

The open-source DESY FPGA firmware framework (FWK) is the backbone of the implementation and soft-verification processes [3]. FWK generates the register abstraction layer using the DesyRDL tool, which serves as an interface for both the ChimeraTK software framework and SIL simulations [4].

THE SETUP FOR INTEGRATION TESTS AND SYSTEM IDENTIFICATION

The FOFB system design for PETRA-IV is flexible to be extended by feedback from other subsystems of the machine and the beamlines. It also supports studies for digital twin and distributed control. However, the initial goal is to build a centralized control strategy, which is highly dependent on the health of data links and the primary nodes of the extended star network topology. To increase availability, each BPM_H will have a redundant data link to the associated LOC, FCM_H will be connected also to the redundant FCM_D, and GOC and LOC nodes will be utilized in a redundant manner. In the event of an internal failure, this feature provides instantaneous switching to the redundant controller path without any downtime. Populating redundant nodes and links enables yet another powerful feature for the machine, namely Built-In Self-Test (BIST). The BIST mode is illustrated in Fig. 5 on the left side. In this mode, the primary

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or secondary parts of the system turn into a plant emulator, while the other parts are used for normal operation and are being tested. Our experience with large machines shows that BIST will not only be useful for pre-commissioning but will also be very valuable during start-up after any maintenance break.

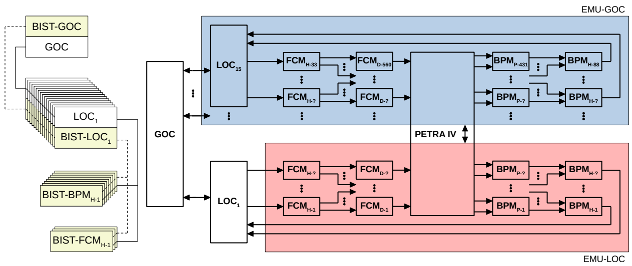

Figure 5: Full-scale real-time emulation.

In addition to the BIST setup, another full-scale real-time emulation setup is under development. The setup, shown in Fig. 5 on the right side, will be used for LOC and GOC prototyping. Plant emulation will be partitioned into two FPGAs for this HIL simulation. The loop will be closed using only a single LOC node together with the GOC, while emulation on one of the FPGAs will include the model of other LOCs.

The BPM signal processing characteristics are of utmost importance for the FOFB system. Previous measurement campaigns using a zero-offset emulator at PETRA-III have provided data to estimate the noise characteristics of the new MircoTCA-based BPM system [5]. To achieve a complete model of the feedback path that covers all modes of operation, a beam emulator is being developed for system identification. This approach allows for the controlled injection of signals throughout the entire feedback path, enabling a comprehensive analysis of the system transfer function, including latencies. It also allows for the quantification of artifacts from the crossbar switching mechanism used for drift compensation, which is crucial for a complete understanding of the system dynamics. The data gathered from these experiments will be indispensable for designing appropriate filters and control strategies to ensure optimal orbit stabilization performance.

Fig. 6 shows the beam emulation setup, which couples a MicroTCA-based multi-channel RF signal generator and a BPM_H to the device under test (DUT). The DUT is a BPM_P with a single external switch matrix. The digital back-end of the RF signal generator is implemented with a deep memory on an Advanced Mezzanine Card (AMC), while the RF front-end is a Vector Modulator (VM) on a Rear Transition Module (RTM). Two sets of this RF signal generator are synchronized via MicroTCA backplane to emulate all 4 channels of a BPM. The setup drives the DUT with the RF signals that would normally be generated by bandpass filtering the beam-induced pulses on the RTM of the BPM_P. Additionally, BPM_H firmware is extended to support an RTM with SFP connections to demonstrate the data link layer protocol latency of the complete chain, starting from BPM_P and looping back to FCM_D.

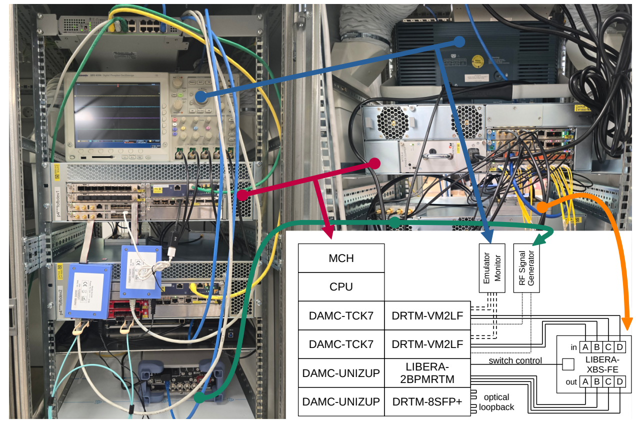

Figure 6: Beam emulation setup.

CONCLUSION AND OUTLOOK

The MBD methodology has been adopted for developing the FOFB system for PETRA-IV. System design is progressing to fine-tune the controller synthesis, and the implementation process has started. The model-based development framework will enable detailed verification and tuning of the implementation.

Demanding controller performance for fourth-generation light sources is only achievable by a deep understanding of the system dynamics and the disturbance characteristics [6]. The external sources of disturbances have been studied and presented previously. The modes of machine operation and interacting subsystem parameters have also been analyzed, modeled, validated, and presented. The consequences of the disturbances in conjunction with machine parameters are studied using empirical models of sensors and actuators. To enhance these empirical models, system identification for the integral parts of the FOFB system is ongoing using real-time emulators.

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