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Development of the CoRDIA detector: first performance estimations

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Abstract: CoRDIA is an X-ray imager being developed for Photon Science experiments at 4th generation Synchrotron Rings. Its goal is to be capable of continuous operation at 150 kframe/s. Its Analog Front-End consists of a battery of adaptive-gain amplifiers and Analog-to-Digital converters, arranged in a pipelined, modular structure compatible with a compact pixel pitch (110 µm). Prototypes have been designed using a 65 nm process and were characterized, confirming expected performance in terms of noise, linearity, and adaptive gain operation at the operational speed. Some shortcomings have been identified and addressed in an improved layout.

Keywords: Front-end electronics for detector readout; X-ray detectors

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Contents

1 Introduction **1**

2 CoRDIA **1**

2.1 First performance estimations 2

2.2 Things to be improved 4

3 Conclusions and future steps **5**

1 Introduction

Several 3^{rd} generation Synchrotron Rings (SRs) are being upgraded to the diffraction limit [1–3], which is expected to improve their brilliance and reduce their emittance. X-ray imagers need to be upgraded to cope with the more intense and more focused beam, while not sacrificing single-photon resolution in the darker areas of the image, and mantaining a compact pixel size not to compromise spatial resolution.

Current X-ray images have frame rates of a few kframe/s (typical examples: [4, 5]), but for future experiments this will need to be increased by 2 orders of magnitude.

The presence of high-intensity areas (such as Bragg peaks), where multiple photons arrive on the same spot at the same time, makes photon detection more complicated than a binary hit/no-hit evaluation -such as could be delivered by a photon-counting detector- and gives a definite advantage to charge-integrating architectures.

While there are detectors for high-repetition rate Free Electron Lasers (HR-FELs) that can take short bursts of images at MHz rates ([6, 7]), these detectors rely on storing images in internal memory and then reading them out at a slow rate: this both inflates the pixel size and introduces a dead time during readout. In contrast, diffraction-limited SRs require continuous high-frame-rate operation (>100 kframe/s). A detector able to operate continuously at high frame rate would also be an interesting option for HR-FELs considering continuous or quasi-continuous operation.

The SR upgrade to the diffraction limit is often coupled with a slight increase in the photon energy, towards the energy range (~40 keV) where silicon is no longer a suitable sensor material, thus compatibility with High-Z sensors is desirable. Since electrons are the prevalent carriers in High-Z materials, an electron-collecting Front-End (FE) is preferable to the more-conventional hole-collecting circuit.

2 CoRDIA

The Continuous Readout Digitising Imager Array (CoRDIA) is a development project of DESY and University of Bonn, aimed at producing a hybrid detector capable of continuous operation at 150 kframe/s (faster than the revolution frequency of the PETRA storage ring). It aims at single photon resolution at 12 keV, combined with a substantial dynamic range, enlarged by an adaptive-gain scheme (1.75 kphotons/pixel/frame, corresponding to ~260 Mcount/pixel/s @150 kframe/s), in a compact pixel size (~110 µm). The readout ASIC is compatible to high-Z sensors for detection of higher energy photons, but most of the description below will refer to response to a charge injection emulating 12 keV photons.

2026 JINST 21 C05011

A description of the readout ASIC architecture has been provided in [8], along with an overview of (some of) the prototypes designed and produced to test the performance of single circuit blocks and circuit chains. We will present here the first performance estimations of the system, mainly extracted from the tests performed on the CoRDIA_02 prototype, which features four "superpixel" structures. Each "superpixel" (grouping of 4×4 pixels) is composed of 16 FE circuits coupled to a Correlated Double-Sampling (CDS) circuit, an ADC to digitize them, and space reserved for the digital streamout circuit, in a 440 µm × 440 µm area (so that it could be fully covered by a 4×4-pixel section of a sensor having a 110 µm pitch). The structures also include 2 programmable calibration circuits (a pulsed-capacitor and a current source) that could be used to inject a charge in the circuit that emulates photogeneration by one or more photons. The FE inputs are redistributed to an uniformly-spaced 2D array of bump-pads to facilitate bonding to a sensor (figure 1).

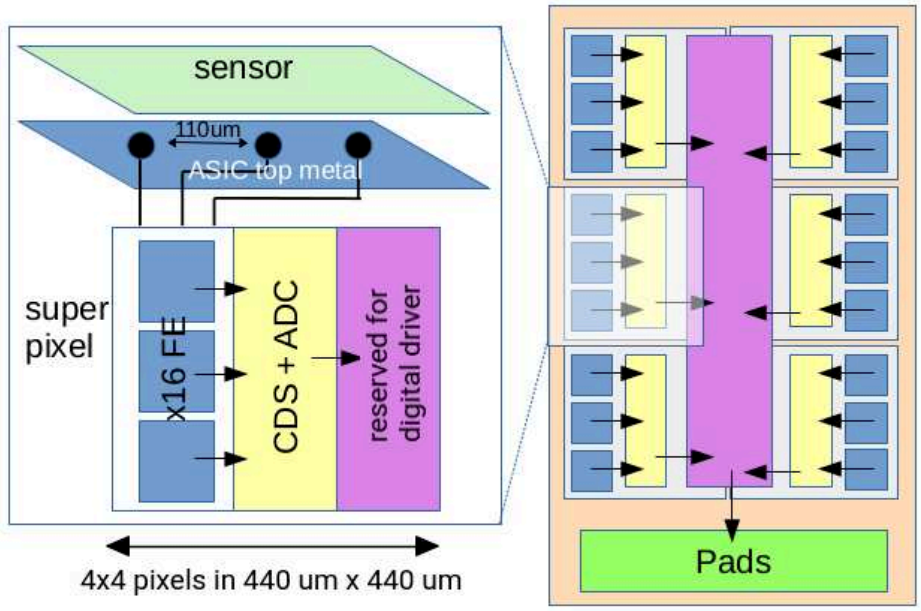

Figure 1. Block diagram describing a "superpixel" unit (grouping of 4×4 pixels) consisting of a set of 16 Front End preamplifiers, a Correlated Double-Sampling (CDS) circuit, an ADC to digitize them, and space reserved for the fast digital driver. The "superpixel" occupies a 440 µm × 440 µm area, and thus can be covered by a 4×4 subarray of a sensor with a 110 µm pitch, with no dead area.

2.1 First performance estimations

We have used a pulsed-capacitor programmable calibration circuit, to inject in our pixels a charge emulating the arrival of photons in a silicon sensor, gradually increasing the injected charge from 0 to 250 (12 keV) photons.

The circuit was read out through the standard data path, with a programmable charge injected by the calibration circuits in the preamplifiers, whose outputs are sequentially fed into the CDS circuit and digitized by the ADC. We recorded the ADC output to evaluate the effect of the injected charge. The circuit was controlled by an FPGA, using the clock frequencies intended for real operation (150 kframe/s for the FE and 2.5 MS/s for the CDS and ADC).

2026 JINST 21 C05011

We were able to characterize the adaptive gain operation of the FE at the target speed (150 kframe/s), pipelined to the superpixel ADC, and to verify that each pixel is able to switch its gain depending on the incoming charge. The high-to-low gain ratio of the adaptive gain circuit was measured to be ~31, which reasonably matches design expectations. The gain switch starts happening for charge injection equivalent to ~50 (12 keV) photons, which again matches design expectations. After calibration, the high-gain and low-gain portions of the detector response align to a single straight line, as expected.

By using both calibration circuits, we extended the charge injection till the end of our linear dynamic range, which was estimated to be about 1.75 kphotons/pixel/frame (corresponding to 260 Mcount/pixel/s), as shown in figure 2. Until that point, the photonized response of the detector closely matches expectations, with deviations mostly within the 1–2% cones. Beyond that range, the system start saturating, and a non-linear calibration would be needed to reconstruct the input charge from the detector output.

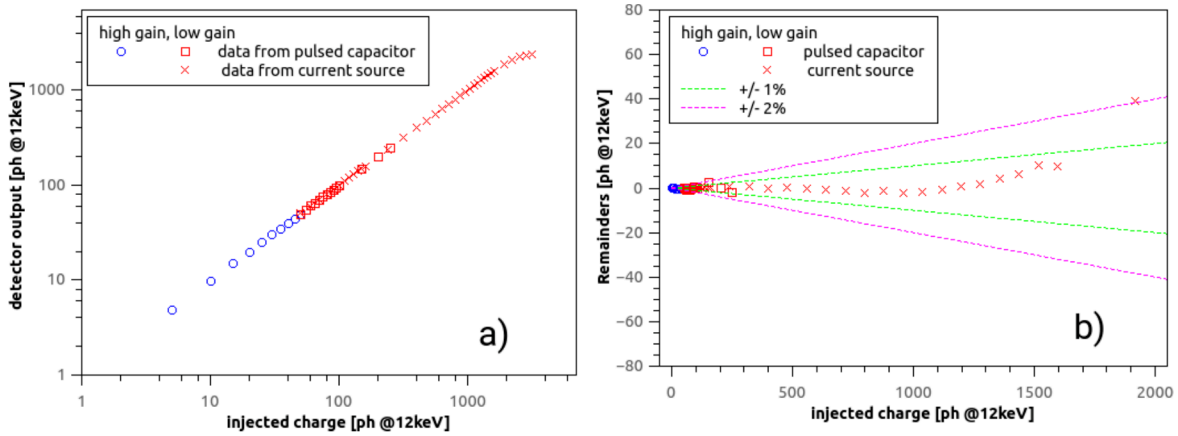

Figure 2. Linear Dynamic Range estimation: each point represents the average value from a 1000-measurements set. After calibration, the circuit is expected to respond linearly to its input, so that the charge injected can be measured by the photonized output. A deviation of more than 2% from the expected value is used as an estimation of the limit of the range where the system responds linearly. (a) Overall behaviour of the detector along the full dynamic range. (b) Deviations from the expected behaviour, calculated as the relative difference between the detector output after photonization and the injected charge as an equivalent number of 12 keV photons. For the pulsed capacitor injection, the charge injected was evalued as the CΔV product (voltage step pulsed across the capacitor connected to the preamplifier input, mutliplied by the capacitor value). For the current source injection, the charge injected was evalued as the IΔt product (current value, multiplied by the time interval during which it was injected into the preamplifier).

For experiments in constant flux condition, we think we can extend the linear dynamic range further, by blinding the sensor for a fraction of the integration period (High Dynamic Range mode), thus reducing charge collection and postponing saturation.

Our estimation of the readout noise of the circuit chain is 255 e, which corresponds to about 7% of the charge photogenerated by a 12 keV photon.

As expected, the noise increases as the adaptive gain circuit reduces the gain, but it remains below the poisson limit for 12 keV photons (figure 3).

2026 JINST 21 C05011

The results are in line with our goals and expectation; it must be stressed, however, that these results should be taken as preliminary, and need to be confirmed once a proper sensor is bump-bonded to the readout ASIC, as the increase of the capacitance at the input of the preamplifier is expected to increase thermal (kTC) noise.

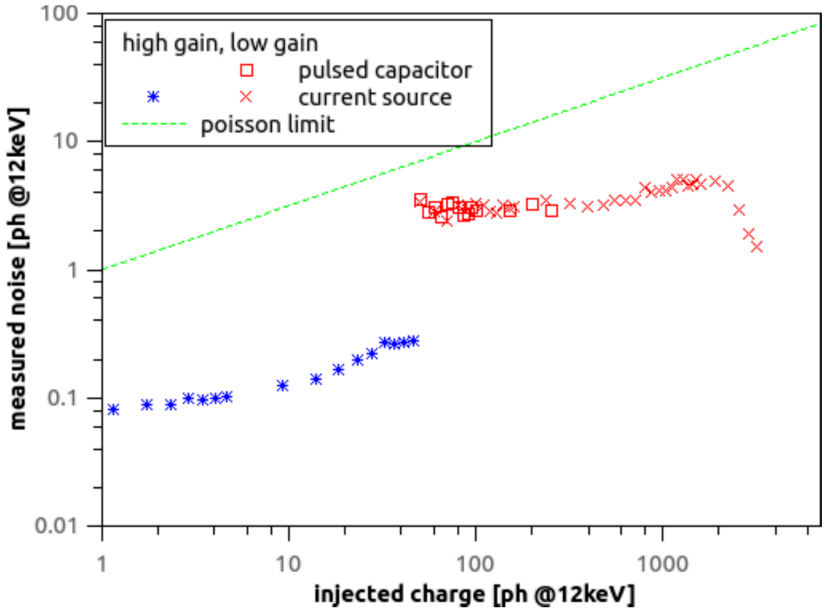

Figure 3. Noise estimation over the dynamic range from the standard deviation of 1000 samples per measurement point. The noise contribution from the calibration sources is included in addition to that of the signal processing chain (preamplifiers to ADC), but the result still remains below the poisson limit.

2.2 Things to be improved

The design and test of chip prototypes was useful to find shortcomings to be corrected before integrating the components in a full-sized chip, in an expensive engineering run.

Tests on CoRDIA_02 prototypes showed occasional cross-talk effects between adjacent pixels: a dark pixel output was sometimes found to be perturbed, when an adjacent pixel was injected with a significant charge.

The cross-talk effects have been traced to insufficient shielding between the pad redistribution layers (connecting the pads facing the sensor to the inputs of the FE circuits) and the Sample/Hold circuits used to locally store the signal to be digitized in the next frame.

By their nature, the pad redistribution layers need to cross pixel boundaries, so that the pad redistribution layer of one pixel might overlap the Sample/Hold circuit of the adjacent pixel. If insufficient shielding is provided between the two, a voltage rise/drop on the Sample/Hold of a pixel (for example, because that pixel is injected with charge) could couple with the pad redistribution layer of the adjacent pixel, perturbing the input of the preamplifier of the adjacent pixel. The effect was reproduced in simulation after a appropriate post-layout parasitic extraction of the cross-coupling capacitances by design tools.

2026 JINST 21 C05011

An improved layout provides better shielding to the pad redistribution network, by means of intermediate layers connected to ground, covering the area. Simulations of the improved layout show a complete suppression of the cross-talk that we had observed on our non-optimized layout (figure 4).

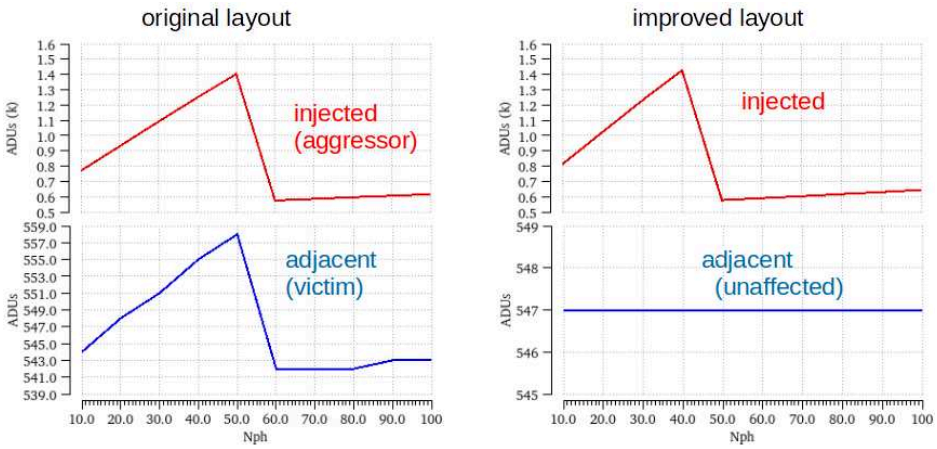

Figure 4. After appropriate extraction of coupling capacitances, the cross-talk effect is reproduced in simulation of the original layout (left). The effect is suppressed in the improved layout (right), which includes improved shielding of critical areas.

Another shortcoming was found during the test of a separate prototype (CoRDIA_03), aimed at the characterization of the fast data streamout circuit. This architecture (developed by NIKHEF for the Timepix4 chip) has been extensively tested by the Timepix collaboration at 5.12 Gb/s [9]. We have not, however, been able to fully replicate these results in our prototype, in which we observed a partially closed eye diagram, and occasional error bursts in data transmission. This has been tracked down in our layout to excessive (10–15 ohm) parasitic resistance of the lines providing power and ground to the fast driver, causing local voltage drops during operation, reproduced in simulation once the parasitic resistances were properly included in the testbench.

A new layout reduces the parasitic resistance by an order of magnitude, introduces substantial (100 pF) decoupling capacitors and improves routing to the pads. A simulation of this new layout results in a complete suppression of the problem observed in the first prototype.

Improved layouts (CoRDIA_03B and CoRDIA_05) are being manufactured and are expected to be tested during 2026.

3 Conclusions and future steps

First performance estimations have been provided for the CoRDIA detector, in terms of adaptive-gain operation at the operational speed, dynamic range, linearity and noise.

Some shortcomings have been observed (cross-talk effects due to insufficient shielding and occasional error bursts in data transmission due to excessive resistance in the power/ground distribution grids), that have been corrected in improved designs.

Our next step will be to test a pixel array demonstrator that will emulate the length of the full-scale chip (~2 cm) to look for, and to solve, eventual voltage drops.

Our objective is to have a full-sized detector ready by the start of operation of the upgraded PETRA-IV SR, expected in 2032.

2026 JINST 21 C05011

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2026 JINST 21 C05011