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Timing performance of the DESY ER1 chip in a 65 nm CMOS imaging technology

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ABSTRACT

Monolithic active pixel sensors (MAPS) are promising candidates for the next generation of vertex detectors at future lepton colliders. One particularly interesting advancement is the recently accessible 65 nm CMOS imaging technology, which offers higher logic density compared to larger feature-size processes, making it highly appealing to the High Energy Physics community. This paper highlights the progress made with prototypes, an analog test structure, DESY ER1, featuring a 2 × 2 active pixel configuration. The chip is integrated into the Caribou DAQ system, and detailed laboratory and test beam characterizations have been conducted. The DESY ER1 provides access to analog waveforms generated by the charge-sensitive amplifier with a Krummenacher feedback loop. The paper presents the initial testing results of DESY ER1 at sensor bias voltage of −3.6 V, including the charge calibration with Fe-55 and tracking performance characterization in test beam. The test beam measurements shows that the time resolution for detecting charged particles is below 8.72 ns at a threshold of 200 e^-.

1. Introduction

The High Energy Physics community is driven by precision measurements of the Standard Model and beyond. Lepton colliders are highly competitive with hadron colliders due to their clean environment after collisions and the use of polarizable beams. To meet the precision goals in lepton colliders, stringent requirements must be met for vertex detectors. Although the specific requirements vary depending on the lepton collider concept, as noted in [1], there are some commonalities. These include excellent spatial resolution, a low material budget, relaxed radiation tolerance, and more. For instance, the vertex detector at CLIC has several key requirements [2]:

- The spatial resolution should be smaller than 3 μm.
- The material budget should be less than 0.1% of the radiation length (X/X_0) per layer to reduce multiple scattering.
- The time resolution should be on the order of a few nanoseconds.
- Power consumption should be less than 50 mW/cm^2 to enable air cooling and further minimize the material budget.

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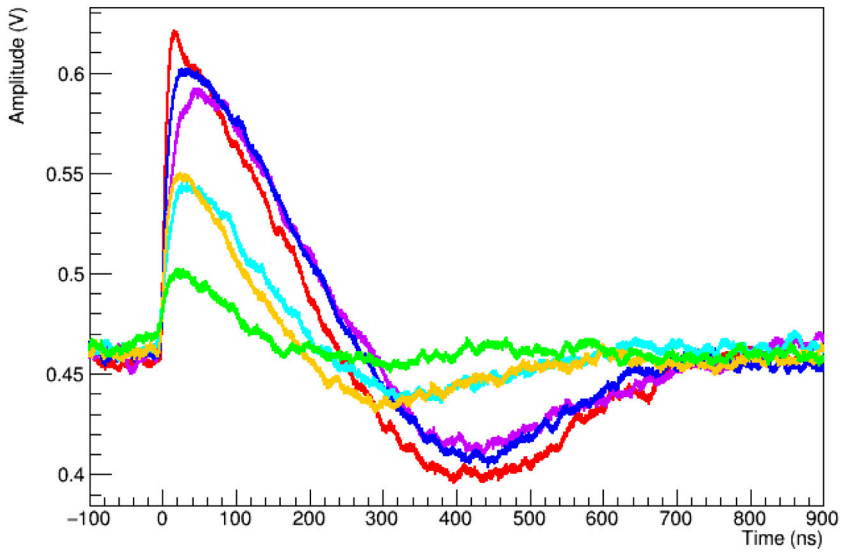
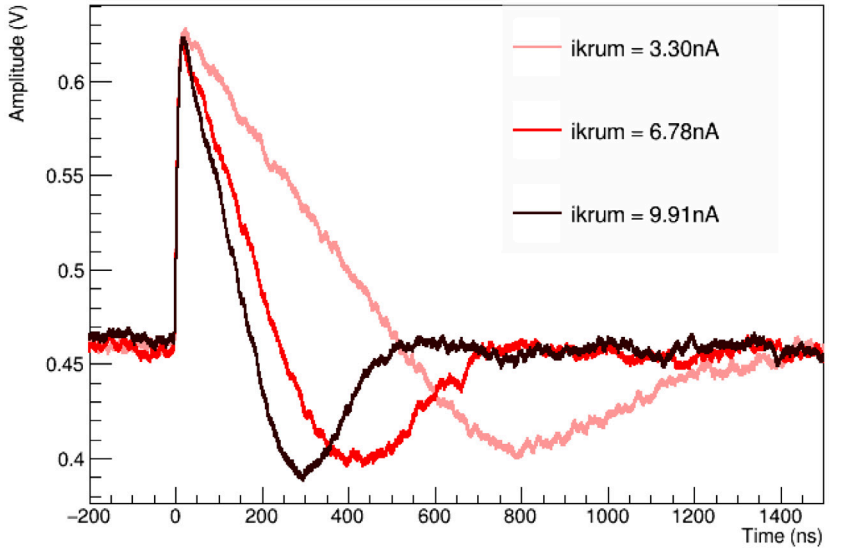


(a)



(b)

Fig. 1. Recorded Fe-55 waveform examples from the top-right pixel with sensor biased at −3.6 V: (a) The chip operated at I_{krum} = 6.78 nA. The selected waveforms have different amplitudes. (b) The chip operated at various I_{krum}. The selected waveforms have the same rise time where the ballistic deficit is minimized.

– The radiation tolerance should be around, after applying a safety factor, 4×10^{10} n_{eq}/cm^2/year and a total ionizing dose of up to 200 Gy/year.

Although the available detector technologies can meet several individual requirements, none can fulfill all of them simultaneously. Therefore, there is a need to explore new vertex detector technologies for future lepton colliders. Furthermore, the reference particle tracking telescopes at test beam facilities must be updated to effectively characterize the next generation of vertex detectors.

Monolithic active pixel sensors (MAPS) integrate both sensor and electronics on a single wafer, allowing for a very low material budget and the possibility of achieving small pixel sizes. As a result, MAPS are highly attractive for the next generation of vertex detectors. One of the innovative technologies in this field is the 65 nm CMOS imaging technology, which is being studied in the context of the CERN EP R&D programme, with active contributions from several international institutes. Recently, this technology was qualified by the ALICE collaboration for the ITS3 project [3], which makes it more promising for future lepton colliders.

Two prototypes are dedicated to future vertex detector design studies, based on the latest common submission [4] of the 65 nm technology: DESY ER1 and H2M. Both prototypes feature a similar sensor layout and analog front-end but serve different purposes. The DESY ER1 is a small analog test structure that allows access to the analog waveform, enabling a detailed understanding of the front-end. While the H2M is a fully integrated chip that has been confirmed to be fully functional and supports four digital acquisition modes with digital processing in each pixel [5]. This paper presents the initial testing results of the DESY ER1, focusing on its timing performance.

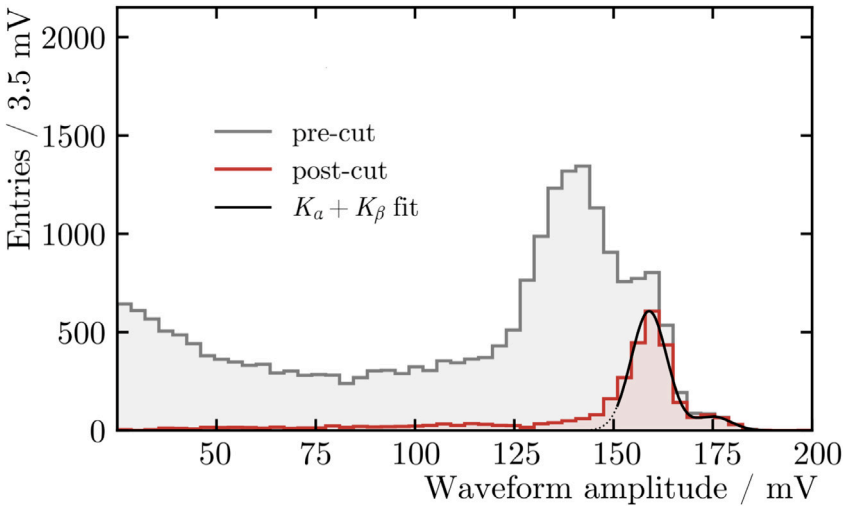


Fig. 2. Example of the Fe-55 spectra from the top-right pixel before and after a rise time cut. The chip operated with I_{krum} = 6.78 nA. A double Gaussian function has been employed to fit the Fe-55 peaks on the post-cut spectrum, which are represented by the black smooth line.

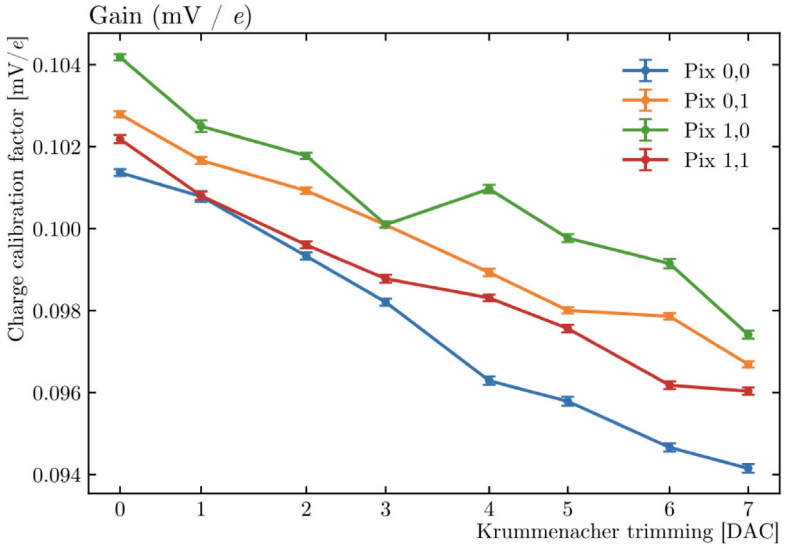


Fig. 3. Charge calibration factors for each pixel of the DESY ER1 chip are functions of the Krummenacher trimming settings in DAC unit. As the Krummenacher trimming setting increases, so does I_{krum}. A trimming setting of 4 DAC corresponds to I_{krum} = 6.78 nA. Pix (0.0) is the bottom left pixel; Pix (1,1) is the top right pixel.

2. DESY ER1 chip

The sensor of DESY ER1 is designed in a modified process that includes a gap in the deep n-type implant, as described in [4]. The pixel size is 35 × 25 μm^2 and the gap size of the tested chip in this paper is 4 μm. Since the available number of wirebond pads on this chiplet is limited, DESY ER1 features a 2 × 2 configuration of active pixels. To prevent boundary effects on the charge collection of these active pixels, there are dummy pixels arranged around them that have the same sensor layout. The analog front-end is a charge-sensitive amplifier utilizing a Krummenacher feedback loop [6]. The Krummenacher biases can be adjusted via the slow control interface. The readout board is specifically designed for processing analog signals and is integrated into a Caribou system [7]. Each pixel's signal waveform is read out synchronously using an oscilloscope, allowing for detailed analysis.

3. Fe-55 measurements

The chip was tested in a laboratory using an Fe-55 source. Fig. 1(a) shows examples of waveforms recorded from the top-right pixel with the Fe-55 source. Other pixels show similar waveforms . The first three largest signals (red, blue and purple) correspond to the complete collection of charges deposited by the X-ray. For signals with a slower rise time (blue and purple), the ballistic deficit [8] is observed. The falling slew rates of these three waveforms are the same, indicating that the ballistic effect has impact on the amplitude measurement but not on the Time-over-Threshold (ToT) measurement at low to moderate threshold regions. The remaining three waveforms represent charge-sharing signals, which exhibit different falling slew rates due to the front-end's non-linear response to a smaller amount of input charges. Fig. 1(b) shows the effects of the Krummenacher current (I_{krum}) by presenting some waveforms recorded when the chip was operated at different values of I_{krum}. The falling slew rate increases with higher I_{krum}, as anticipated, because the ToT gain of the front-end is designed to be inversely proportional to I_{krum}.

To obtain reliable charge calibration results and avoid bias from the ballistic deficit, a cut is applied to the rise time of waveforms from Fe-55 source measurements to select the faster signals. The total jitter contribution to the rise time is approximately 212 ps, according to front-end studies. Waveforms with a rise time three times 212 ps further from the peak are rejected. Fig. 2 shows an example of the Fe-55 spectra from the top-right pixel before and after a rise time

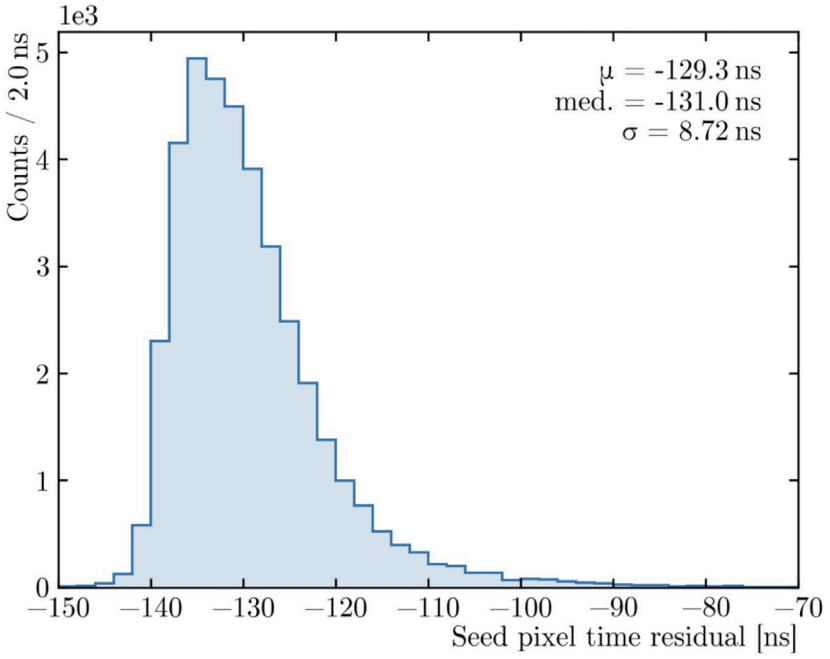


Fig. 4. Preliminary ToA distribution of all hits on the DESY ER1 chip with an associated telescope track. The threshold is at 200 e^-.

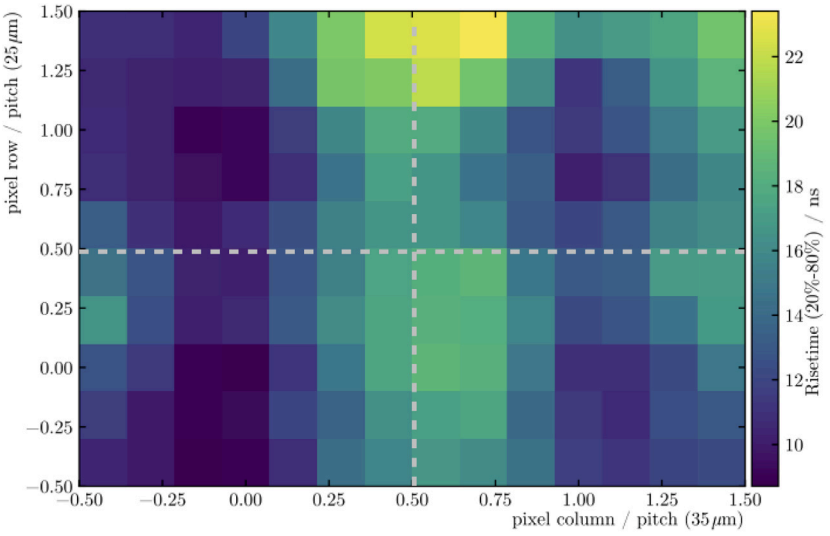


Fig. 5. Preliminary rise time map of the DESY ER1 chip from test beam analysis. The threshold is at 200 e^-.

cut. With the rise time cut, the Fe-55 peaks have been resolved, and a double Gaussian function was used to fit these peaks. The fitting results for the Fe-55 K_α peak were employed to determine the charge calibration factor of the front-end. Fig. 3 shows the charge calibration factor for each pixel as the function of I_{krum}. The calibration factors are consistent across the pixels, with less than 10% variation. Notably, the factor decreases as I_{krum} increases as expected from the front-end design.

4. Testbeam measurements

The DESY ER1 chip was also tested with a 3.6 GeV electron beam at the DESY II test beam facility [9]. The ADENIUM telescope [10], which consists of six detector planes, was used to reconstruct reference tracks. The pointing resolution of the telescope was estimated to be 4.3 μm. The chip was placed in the middle of the telescope planes. At the end of the telescope, `TelePix2` [11], was employed to generate region-of-interest triggers and served as the timing layer. The sensor of DESY ER1 was biased at −3.6 V. The top-right pixel operated at a current of I_{krum} = 2.32 nA, while the other three pixels operated at I_{krum} = 3.30 nA. This choice of I_{krum} was made to achieve a similar falling slew rate among the pixels for ToT measurements, which are not included in this paper. The amplitude of the waveforms was converted to the charge equivalent unit using the calibration factors obtained in the previous section. A threshold of 200 e^- was applied during the test beam analysis to eliminate noise contamination and retain as many signal waveforms as possible. Given the small size of the chip, the data-taking time needed to be extended to more than a day to gather sufficient events for analysis. To account for minor changes in the chip's position due to thermal expansion during the prolonged data-taking period, a time-dependent alignment method [12] was applied. The spatial resolution of the chip is determined by subtracting the pointing resolution of the telescope and the uncertainty due to thermal expansion from the standard deviation of the residuals between the

chip clusters and their reference tracks. The spatial resolution of the chip is calculated to be 10.65 ± 0.08 μm in the long direction and 8.38 ± 0.07 μm in the short direction, which are worse than the predicted limit of pitch/ $\sqrt{12}$. One possible reason for this discrepancy is that the printed circuit board (PCB), which contains a metal trace, runs directly beneath the chip. This could locally increase the material budget and, in turn, degrade the expected track resolution.

Fig. 4 illustrates the distribution of time residuals for seed pixels across all hits on the DESY ER1 chip that are associated with telescope tracks. The time residual is defined as the difference between the Time-of-Arrival (ToA) of the waveforms measured at a threshold of 200 e^- and the time corresponding to the associated tracks. The standard deviation of the time residual distribution includes contributions from both the chip, the TLU binning uncertainty and `TelePix2` time resolution. The TLU binning resolution is $0.718/\sqrt{12}$ ns [13]. The time resolution of `TelePix2` is measured to be smaller than 3.84 ns [11]. Thus, the time resolution of the chip is constrained to be in [7.84 ± 0.03 ns, 8.72 ± 0.03 ns]. The tail extending towards larger time residuals is primarily influenced by waveforms with smaller amplitudes. When the threshold is increased to 330 e^-, the time resolution is reduced by 30%.

Fig. 5 illustrates the in-pixel rise time map. Here, the rise time is defined as the duration it takes for the waveform to change from 20% to 80% of the amplitude. In contrast to the Fe-55 measurements, no rise time cut was applied to obtain the complete matrix rise-time map. It is observed that the rise time is asymmetric, varying within a pixel, between pixels, and also in the row and column directions. This variation is assumed to result from a combination of the rectangular pixel shape and subtle effects from the n-well structure and its position. The latter effect has also been observed and discussed in [5,14] and is expected to be more pronounced with a faster front-end and larger pixel pitch.

5. Summary and outlook

The DESY ER1 prototype is built on 65 nm CMOS imaging technology and offers access to analog waveforms, allowing the examination of the characteristics of the charge-sensitive amplifier with Krummenacher current feedback. Charge calibration has been conducted using Fe-55 and the chip has been characterized using charged beam particles. The time resolution for detecting charged particles is measured to be smaller than 8.72 ns at a threshold of 200 e^-. Together with the H2M chip, they represent the initial exploration of this technology, integrating a large pixel size with a fast front-end. To fully utilize the capabilities of the DESY ER1 chip, numerous studies and in-depth investigations are currently underway, including time-over-threshold measurements and tracking efficiency studies.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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