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Full Length Article

Characterisation, simulation and test beam data analysis of stitched passive CMOS strip sensors

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ABSTRACT

In the passive CMOS Strips Project, strip sensors were designed at the University of Bonn and produced by LFoundry in 150 nm technology, with an additional backside processing from IZM Berlin. Up to five individual reticules were connected by stitching at the foundry in order to obtain the typical strip lengths required for the LHC Phase-II upgrade of ATLAS or CMS trackers. Sensors electrical properties were simulated using Sentaurus TCAD and the results were compared to experimentally measured data. Detector modules were also constructed from several sensors and thoroughly studied in two beam campaigns at DESY. All of these measurements were performed before and after irradiation. This contribution provides an overview of simulation results, its comparison to measured data and in particular presents first test beam results for irradiated and unirradiated passive CMOS strip sensors. We are demonstrating that large area sensors with sufficient radiation hardness can be obtained by stitching during the CMOS process, and presenting our plans for the next submission in the framework of this project.

1. Introduction

High-energy particle physics experiments require large area, cost-effective and precise detectors that can operate in radiation-rich environments. CMOS pixel technology has recently proven that it can produce radiation tolerant particle detectors suitable for the tracking layers of collider experiments (STAR, ITS2, MALTA,FCC-ee). The widely commercially used CMOS technology offers an interesting alternative to strip sensors currently being manufactured in microelectronics foundries. The CMOS processes also bring an option to combine the active detection layer and the readout electronics into a single device, allowing for a significant decrease of the material budget used in future tracking detectors (FCC-ee, ITS3, EIC).

This contribution presents passive stitched CMOS silicon strip sensors and investigates their qualities by various experimental techniques, aiming to show that silicon strip sensors can also be fabricated using CMOS technology with no negative impact on their performance.

2. CMOS strip sensors

Passive CMOS silicon strip sensors were fabricated by LFoundry [1] in a 150 nm process. The sensors with p-type bulk are diced from an eight inch wafer with a resistivity of 3–5 kΩ cm, have a nominal active thickness of (150 ± 10) μm and a strip pitch of 75.5 μm. On the backside of the sensors a p^+-implant is implemented, accompanied by homogeneous metal layer below the implant.

A 1 cm^2 reticule was used in the fabrication process, so in order to achieve the desired strip lengths 2.1 and 4.1 cm the sensors had to be stitched. Each sensor has up to five stitches and includes three

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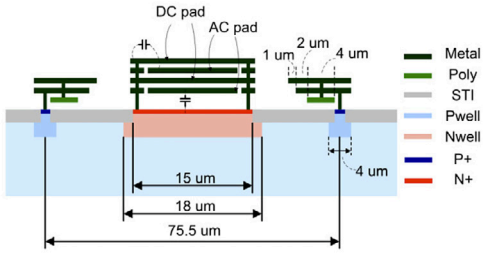
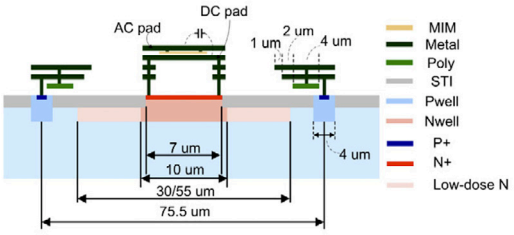


(a) *Regular* design



(b) *Low dose 30/55* design

Fig. 1. Sketch of the CMOS strip implant designs [2].

different designs - *regular, low dose 30* and *low dose 55*. The *regular* has a 15 μm wide strip n^+-implant. The *low dose* designs introduce an additional low-doped n-implant and a MIM capacitor. The low-doped n-implant comes in two widths (30 and 55 μm) and is placed below the high-doped n-implant that for *low dose* designs is only 7 μm wide. The different designs are sketched in Fig. 1.

3. TCAD simulations

In order to investigate our sensors in detail, simulations of the silicon structure using the Sentaurus TCAD [3] simulation software were carried out. After obtaining the model of our structure by simulating the fabrication process step-by-step, we were able to simulate both the microscopic and macroscopic characteristics of all three different designs. The microscopic characteristics, such as electric field and electrostatic potential, provide a detailed look on the differences in the designs, and thanks to the macroscopic characteristics a verification of the experimentally measured values is available. Each of the three different designs was simulated separately as a 1 μm long strip segment. For all simulations the sensor is biased from the backside with ground connected to the n-implant.

Thanks to the simulations, we are able to investigate the electric field of each design in detail. Fig. 2 displays different electric field shapes at the centre of the strip for the three different designs. While for the *regular* design the electric field is higher right below the strip, the *low dose 30* and *low dose 55* show bottom electric field values below the strip. As an effect of the additional low-doped n-implant for the *low dose 30* and *low dose 55* design, the region of higher electric field below the strip spreads through the entire strip width.

For the macroscopic characteristics we are comparing the simulated quantities such as the leakage current, bulk capacitance and interstrip capacitance to the measured values on real structures. All the listed quantities show a very good agreement between measured and simulated data.

Both the simulated and measured values of the leakage current are in the order of nA. The measured IV curves have shown some instabilities and even early breakdowns [4], while for the simulated

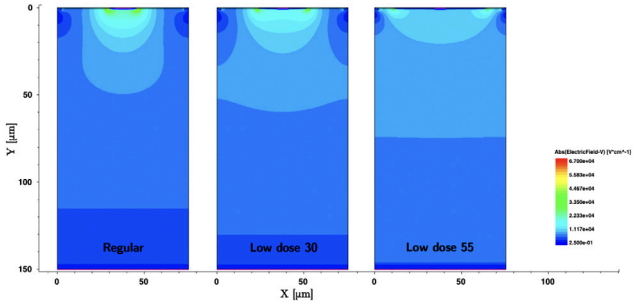


Fig. 2. Electric field of a one strip structure at 100 V for the different designs - *regular, low dose 30* and *low dose 55*.

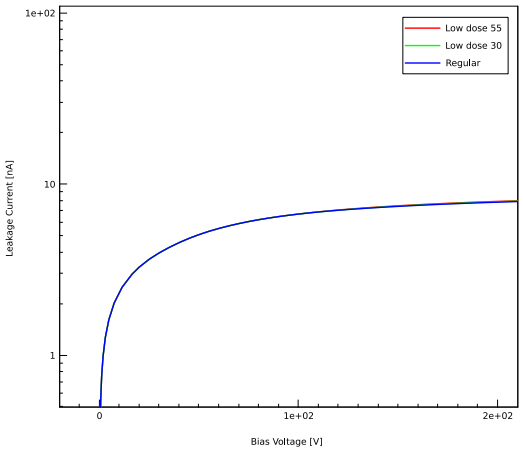


Fig. 3. Simulated leakage current as a function of the bias voltage for the different designs - *regular, low dose 30* and *low dose 55*.

dependencies of the leakage current on the bias voltage the sensor behaviour is that of an ideal silicon structure (see Fig. 3).

The bulk capacitance depends on the number and the length of measured strips. To be able to directly compare the simulated and measured values of bulk capacitance, the simulated 1 μm long strip has to be multiplied by the real strip length (2.1 cm for the short, 4.1 cm for the long sensor), and as there are 40 *regular* and 20 *low dose* strips on each structure, we are also multiplying the simulated bulk capacitance by their number. The resulting simulated bulk capacitance is similar to the measured one. Values of 50 pF for the short strips (2.1 cm) and 100 pF for the long strips (4.2 cm) are measured once full depletion is achieved. Simulated CV curves are plotted in Fig. 4. Focusing on the results of simulations, we observe the highest value of bulk capacitance for the *low dose 55* and the lowest for the *regular* design.

The interstrip capacitance was both measured and simulated using a frequency of 500 kHz and the interstrip capacitance values shown in Fig. 5 are the averages of measured/simulated values between 50 and 80 V. The best agreement between simulation and measurement is for the *low dose 55*, while for the *regular* and *low dose 30* the simulated values slightly overestimate the measured ones.

4. Test beam results

Test beam campaigns were performed in 2022 and 2023 at the DESY-II test beam facility exploiting the 3.4 and 4.2 GeV electron beam line to characterise the CMOS strip sensors in terms of their spatial resolution and hit detection efficiency. Six pixel telescope planes were used to study the Device Under Test (DUT), either unirradiated or irradiated CMOS strip sensors, mounted in a cold box. Behind the

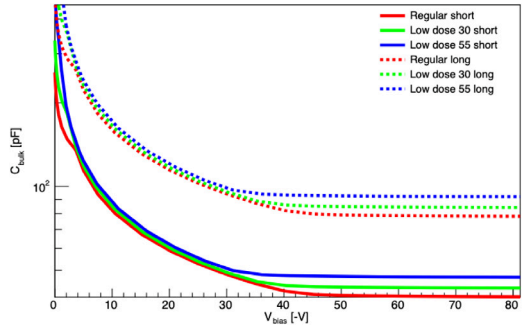


Fig. 4. Simulated bulk capacitance as a function of the bias voltage for the different designs - *regular, low dose 30* and *low dose 55*. Bulk capacitance is plotted for both the short (2.1 cm) and long (4.1 cm) sensors.

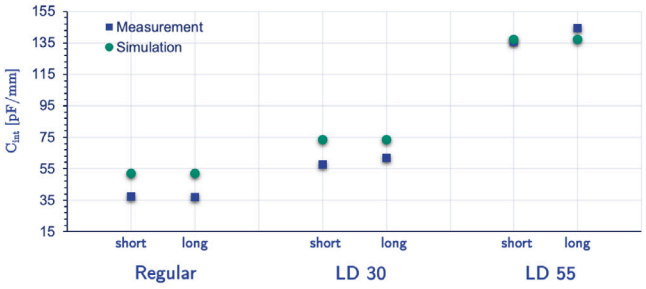


Fig. 5. Comparison of experimentally measured and simulated interstrip capacitance for the different designs - *regular, low dose 30* (LD 30) and *low dose 55* (LD 55).

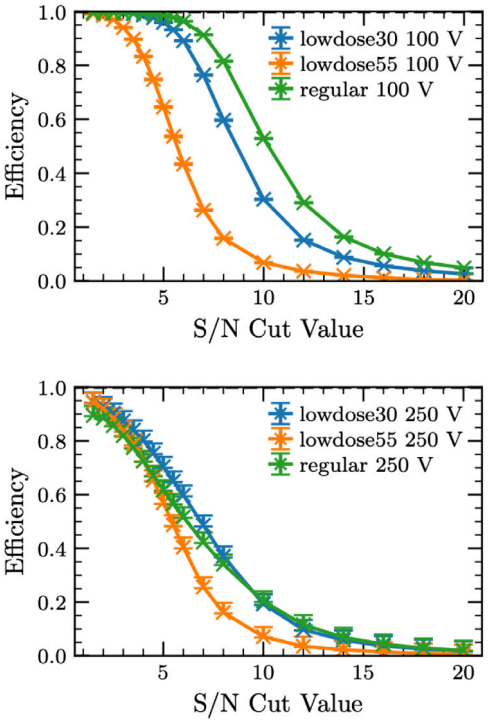


Fig. 6. Efficiencies of the *regular*, *low dose 30* and *low dose 55* design as a function of the signal/noise cut value for an unirradiated sensor (top) and for a neutron irradiated sensor $\Phi_{eq} = 3{\cdot}10^{14}$ n_{eq}/cm^2 (bottom).

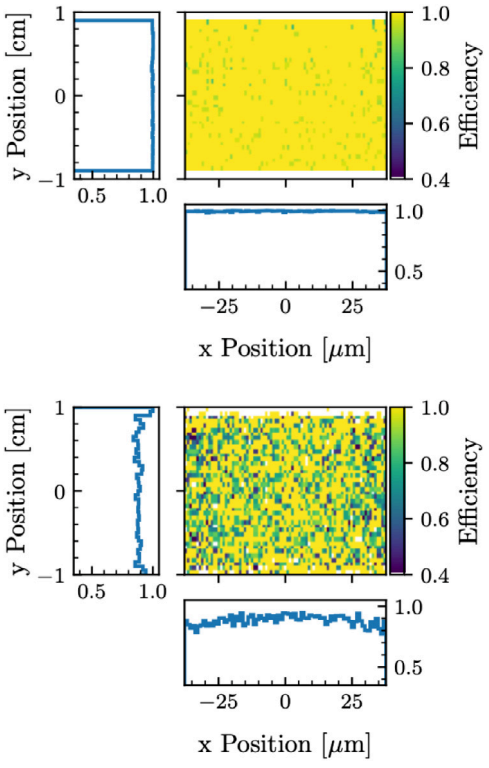


Fig. 7. In-strip efficiencies of the *low dose 30* design as a function of position for an unirradiated sensor (top) and for a neutron irradiated sensor $\Phi_{eq} = 3{\cdot}10^{14}$ n_{eq}/cm^2 (bottom).

telescope layers, a scintillator provided the trigger for the trigger logic unit. The DUT data were recorded by the Alibava system [5].

All three designs of the CMOS strip sensors show the expected shape of the dependence of the efficiency on the signal/noise cut value when unirradiated. As shown in Fig. 6, the unirradiated sensors follow the s-curve shape with a plateau close to one for small to medium seed cuts, a steep descent for further increasing cuts and finally a slow decline towards zero for even higher cuts. On the other hand, for irradiated sensors the efficiency plateau disappears and the dependence on signal/noise cut value only shows the steep decrease and the following slow decline. A clear deterioration in efficiency after irradiation can be observed for all three designs.

The in-strip efficiency allows to investigate any features influencing the hit detection efficiency. For the unirradiated *low dose 30* design a consistent efficiency close to 1 over the entire area was observed with no effects of stitching visible along the strip length. Only small fluctuations of the efficiency can be seen in Fig. 7, due to limited available statistics, inherent to most test beam measurements. After irradiation by 23 MeV neutrons to $\Phi_{eq} = 3{\cdot}10^{14}$ n_{eq}/cm^2, the overall efficiency decreases as the noise is increasing and the collected charge is decreasing due to irradiation. Furthermore, a minor decrease of the efficiency towards the interstrip region is visible due to the irradiation-induced noise increase and signal decrease. This means that hits near the boundary between two strips, which would result in two-strip clusters, are less likely to be reconstructed compared to hits directly onto the strip. Most importantly, no changes in the in-strip efficiency along the stitching lines are observed.

5. Conclusions

Passive CMOS strip sensors, produced using a stitching process to achieve the desired strip lengths, were evaluated before and after irradiation. A detailed look into the sensors electrical characteristics was provided by TCAD simulations and their comparison to measured data. A good agreement of measured values and results of the simulations was observed. As a result of the first test beam data analysis, we do

not see any deterioration in detection efficiency due to the stitching, either before and after irradiation.

The CMOS process is a promising candidate for future experiments needing to cover large areas with silicon detectors for tracking, as stitching shows no effects on the sensor performance. CMOS strips sensors offer a robust and cost-effective solution with satisfactory spatial resolution and less requirements on the data acquisition and read-out electronics.

Further studies of radiation hardness of the examined sensors are needed, and in order to fully benefit from the CMOS technology, a new active sensor design with readout electronics implemented into the same substrate is in preparation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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