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Experiences and lessons learned from the End-of-Substructure card production of the ATLAS ITk Strip upgrade

L. Bauckhage[a,b,*] **A.L. Boebel**,[a] **H. Ceslik**,[a] **M. Dam**[d] **A. da Silva**,[a] **S. Diez Cornell**[a] **C.M. Garvey**[c] **R.S. Gotfredsen**,[d] **P. Göttlicher**,[a] **I.M. Gregor**[a,b] **J.M. Keaveney**[c] **A. Palmelund**,[d] **S. Ruiz Daza**[a,b] **S. Schmitt**[a] **M. Stanitzki**[a] **and L.R. Strom**[a]

[a] *Deutsches Elektronen-Synchrotron DESY, Notkestraße 85, 22607 Hamburg, Germany*
[b] *Physikalisches Institut, University of Bonn, Nußallee 12, 53115 Bonn, Germany*
[c] *Department of Physics, University of Cape Town, Rondebosch, Cape Town 7700, South Africa*
[d] *Niels Bohr Institute, University of Copenhagen, Blegdamsvej 17, 2100 København, Denmark*

E-mail: lukas.bauckhage@desy.de

Abstract: The silicon tracker of the ATLAS experiment will be upgraded for the upcoming High-Luminosity Upgrade of the LHC. The main building blocks of the new strip tracker are modules that consist of silicon sensors and hybrid PCBs hosting the read-out ASICs. The modules are mounted on rigid carbon-fiber substructures, known as staves in the central barrel region and petals in the end-cap regions, that provide common services to all the modules. At the end of each stave or petal side, a so-called End-of-Substructure (EoS) card facilitates the transfer of data, power, and control signals between the modules and the off-detector systems. The EoS connects up to 28 data lines to one or two lpGBT chips that provide data serialization and uses a 10 Gbit s^{-1} versatile optical link to transmit signals to the off-detector systems. To meet the tight integration requirements in the detector, several different EoS card designs are needed. The power to the EoS is provided by a dedicated dual-stage DC-DC package providing 2.5 V and 1.2 V to the EoS cards. As the EoS production of almost 2000 EoS cards and accompanying DC-DC converters is getting close to completion, the production experience including detailed QC statistics and design validation (QA) results is reported on.

Keywords: Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

*Corresponding author.

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Contents

1 Introduction

The ATLAS Experiment at the Large Hadron Collider (LHC) [1] at CERN is preparing for the High-Luminosity LHC (HL-LHC) upgrade planned for the LS3 phase 2026–2030. The increased pile-up and radiation levels at the HL-LHC require a complete replacement of the current Inner Detector (ID) with a new Inner Tracker (ITk) [2]. Part of it is a silicon microstrip (ITk Strip) detector, that will be installed in the central barrel and end-cap regions of the ATLAS detector. End-of-Substructure (EoS) cards are the interface to the links connecting the module front-end electronics to the off-detector systems [3]. Approximately 2000 EoS cards are produced and undergo a detailed quality control procedure. In section 2 the design of the EoS cards is described. The QC procedure is described in section 3. In section 4 the current production and QC status is reported and a selection of recent QC results are discussed in section 5.

2 Design of EoS cards

The ATLAS ITk pixel and barrel and endcap strip detectors are illustrated in figure 1. The ITk Strip detector consists of staves in the barrel and petals in the endcap regions, housing modules with silicon sensors and readout ASICs and an EoS card glued on the end of each substructure [4]. The EoS cards are designed to transfer data, power, and control signals between the modules and the off-detector systems.

Figure 2 gives an overview of the functional components of an EoS card. The EoS card connects up to 28 data streams at 640 Mbit s^{-1} (eLinks) from the modules to the ePorts of one or two low-power Gigabit Transceivers (lpGBT) [5], radiation-hard ASICs developed at CERN. These are multiplexed to 10 Gbit s^{-1} signals and converted to optical signals by Versatile Link Plus (VL+) Transceivers (VTRx+) [6]. Clock and Control signals from off-detector systems are received via a 2.5 Gbit s^{-1} optical fiber. One of the EoS cards is equipped with a dual-stage DC-DC converter that provides 2.5 V and 1.2 V to both EoS cards. Further details on the design of the EoS cards can be found in [7].

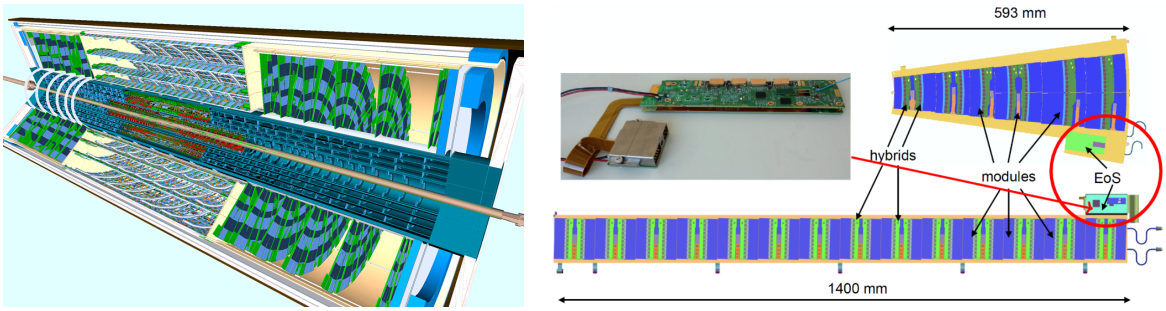

Figure 1. Left: the ATLAS ITk detector overview. Reproduced from [2]. CC BY 4.0. Right: detailed view of petal and stave substructures with the positions of EoS cards marked.

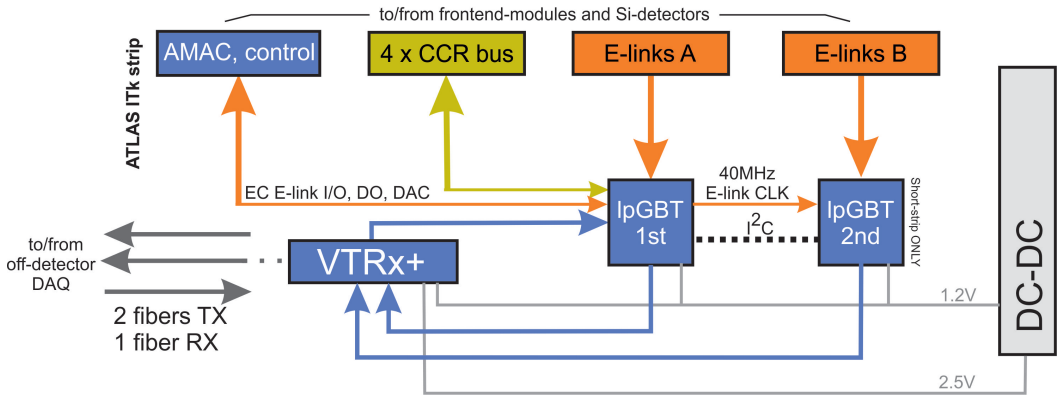

Figure 2. Diagram of components of an EoS card.

3 Quality control procedure

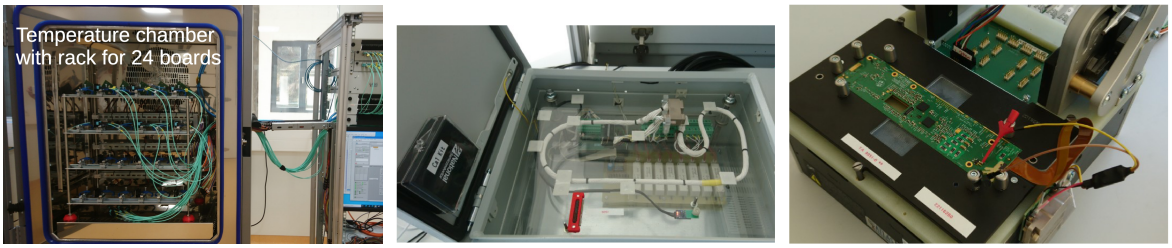

Figure 3. Test setups used for QC. Left: climate chamber with rack of 24 EoS cards. Center: HV test setup. Right: needle prober for electrical and optical connection tests.

The EoS cards undergo a detailed QC procedure to ensure their functionality and reliability. A failure can affect the performance of an entire stave or petal. The QC procedure includes tests of the PCBs using customer testcoupons (CTC) before PCB population, optical and flying probe tests at the production workshop, 3D X-ray imaging of the lpGBT ballgrid arrays (BGA) and four testbenches testing the fully assembled EoS cards. Pictures of the last three testbenches are shown in figure 3. In the first testbench, optical images and infrared (IR) images of the lpGBT and VTRx+ during operation are taken. Bending of cards is identified by flatness measurements and basic electrical tests are performed. The second testbench can test up to 24 EoS cards on a rack in a climate chamber.

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Full functionality tests are performed during ten cycles at −35 °C and 25 °C. The third testbench ramps up the voltage on every HV line separately to 1.1 kV and measures the leakage current. The fourth testbench is a needle prober connected to a FPGA that sends and receives data to and from the EoS card via the VTRx+ and dedicated test pads close to the bond pads connecting the eLinks to the bustape. Bit-Error-Rate-Tests (BERT) are performed on all eLinks and eye diagrams are recorded on the two 10 Gbit s^{-1} up-links and the 2.5 Gbit s^{-1} down-link. The FPGA counts the frame errors on the 10 Gbit s^{-1} up-links via the Cyclic Redundancy Check (CRC) checksum and the lpGBT has a counter for forward-error corrections (FEC) used to compensate bit-flips in the datastream from off-detector to lpGBT on the 2.5 Gbit s^{-1} down-link.

4 Production and QC status

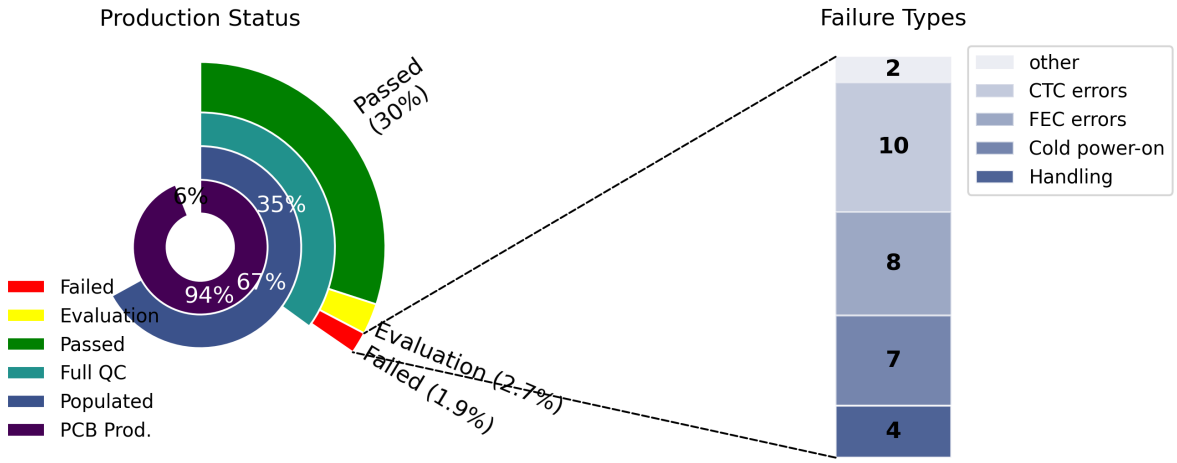

Figure 4. EoS card production and QC status (left) and encountered failure types (right). 1.9 % of all EoS cards (≈ 5 % of all fully-tested EoS cards so far) failed the QC and 2.9 % (≈ 8 % of the fully-tested cards) are marked for "evaluation".

The current status of the EoS card production and QC is summarized in figure 4. The PCB production is almost complete and the population of 2/3 of all EoS cards is done. More than a third of all EoS cards have undergone the full QC so far. However, more than 5 % of these fully-tested EoS cards have failed the QC and 8 % are marked for "evaluation" for different, less critical reasons. Among the most common failure types are, besides handling errors and PCB issues found during the CTC tests, FEC errors and problems of the lpGBT starting up at low temperatures ("cold failure").

5 QC results

5.1 FEC errors

During the BERT tests in the fourth testbench, some EoS cards show a non-zero FEC counter. These are correlated to asymmetric eye diagrams as shown for three examples in figure 5. The eye diagrams of the EoS cards with FEC errors show asymmetric amplitudes to both very high or very low values. These errors are related to an internal DC-offset of the receiver circuit within the lpGBT.

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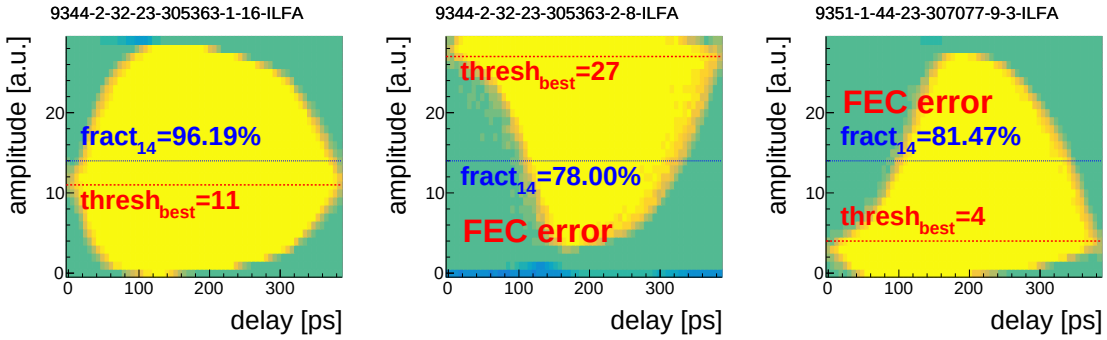

Figure 5. Eye diagrams of a fully functioning EoS card (left) and two EoS cards with FEC errors (center; right). The eye diagrams are recorded using dedicated design blocks in the lpGBT. A discriminator with fixed threshold (near an amplitude of 15) digitizes the data stream and recovers the clock which is input to a PLL. For recording the eye diagram, the threshold of an independent discriminator (vertical axis) is varied, as well as the phase of the discriminator output relative to the PLL clock (horizontal axis). The color coding shows the number of detected logic transitions for a fixed gating time.

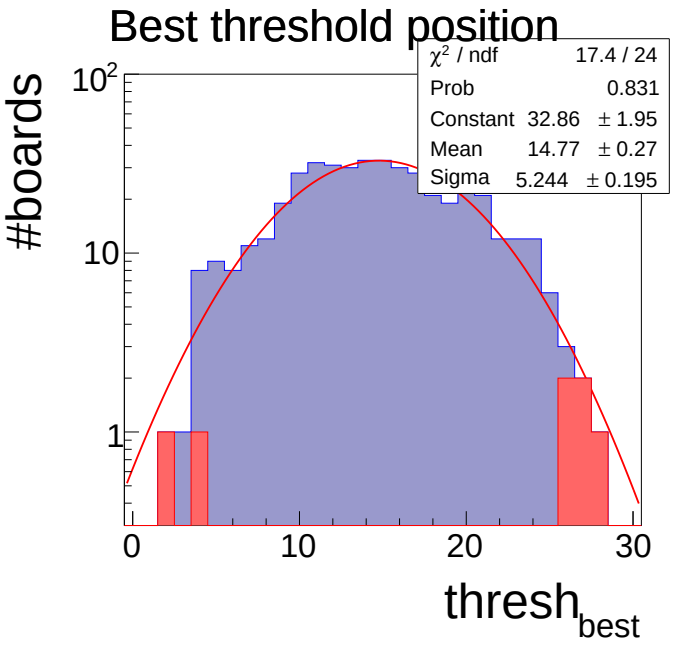

Figure 6. Distribution of the vertical position of the widest horizontal opening of the eye diagram $\text{thresh}_{\text{best}}$ (marked red in figure 5) for all tested EoS cards (blue) and cards with FEC errors (red) and a fitted Gaussian distribution (red) with a standard deviation of $\sigma = 5.2(2)$ around $\mu = 14.8(3)$.

Figure 6 shows the distribution of the vertical position $\text{thresh}_{\text{best}}$ of the widest horizontal opening of the eye diagram (figure 5) for all tested EoS cards and all cards with FEC errors. Cards with FEC errors and asymmetric eye diagrams have very large or very small values of $\text{thresh}_{\text{best}}$. All cards with FEC errors lie more than 2σ away from the mean of the distribution of all tested cards. Based on this variable, a new QC criterion is being developed to identify EoS cards prone to develop FEC errors.

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5.2 Startup in cold

Some EoS cards fail to start up at low temperatures in the climate chamber. The failure is not reproducible at room temperature. Some EoS cards fail to start up at every temperature cycle at −35 °C, while others are able to start in some cycles. When in the error state the card does not react to reset-signals or other means of communication. The power consumption is static but varies between different power cycles. There is a suspicion [8] that the internal clock system of the lpGBT is interrupted.

6 Summary and outlook

CERN-EP-ESE has confirmed that there are lpGBT design issues, which can explain both the appearance of FEC errors and the cold startup problem. These issues could only be identified due to the detailed QC procedures and with a sufficiently large number of EoS cards tested. The EoS card production has been stopped temporarily, while the QC of the remaining already populated cards is ongoing.

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