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Development of CoRDIA: An Imaging Detector for Next-Generation Synchrotron Rings and Free Electron Lasers

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Abstract. CoRDIA (Continuous Readout Digitizing Imager Array) is a hybrid pixel detector development targeted to 4^{th} generation synchrotron sources and (continuous) high-rate Free Electron Lasers. Serving the latter it builds upon the concept of the AGIPD detector, employing a charge sensitive preamplifier with adaptive gain switching. The further signal path comprises of a Correlated Double Sampling stage and an 11 bit Analogue to Digital Converter (ADC), serving a sub array of 16 pixels. 128 ADCs connect to a multi-gigabit serial link to drive the images off chip. For this part CoRDIA adopts the "*GWT-CC*" implementation on the Timepix4 chip by Nikhef. A chip with 256×192 pixels will implement 24 of these blocks. Since the links conform to industry standards (IEEE 802.3ae), the subsequent data acquisition can be based on commercial components.
Performance targets are a continuous frame rate of ≈150 kHz, single-photon sensitivity at <12 keV, and a dynamic range of a few thousand photons (@ 12 keV) with a silicon sensor. The energy range could be extended using active sensors or sensors from "*high-Z*" materials towards lower and higher photon energies.

1 Introduction

Today's detectors for Photon Science X-ray experiments are roughly divided between the ones optimized for Synchrotron Rings and low-repetition-rate Free Electron Lasers (FELs) and the ones optimized for burst mode high-repetition-rate FELs, especially the European XFEL [1]. Detectors in the first category are typically capable of continuous acquisition up to a few kilo-frame/s (typical examples: [3, 4]). A common approach for detectors in the second category ([5, 6, 7]) is to acquire and store a sequence of a few hundred images at MHz rates on the readout ASIC and read out the data at lower speed in the gap between subsequent pulse trains. Due to the on-chip storage, the pixel pitch of these detectors are 200 . . . 500 µm, i.e. relatively large.
The current or planned upgrades of most radiation sources – for Free Electron Lasers towards faster continuous operation at a few 100 kHz, and for synchrotron rings towards the diffraction limit, require a new generation of detectors to profit from this step. For diffraction limited sources like PETRA IV [2] an increase in photon flux by two orders of magnitude is expected compared to PETRA III. To cope with this increase, an increase of the frame rate by that factor with respect to current systems can be derived as a basic specification.

2 CoRDIA Design Goals

CoRDIA will be a modular hybrid pixel detector, suitable for multi-megapixel systems. To complement the already ongoing developments of photon counting detectors for 4^{th} generation sources (e.g. TEM-

PUS [8]), and to also cater for CW[1] XFEL's, the charge integrating principle was chosen. In addition a pixel size of 110 µm × 110 µm was selected for an improved resolution wrt. the ≥200 µm pitch of the present detector systems at the European XFEL.
We aim at sensitivity for single photons (at E_γ<12 keV), and a dynamic range of up to 10 k photons at 12 keV. The dynamic range of a charge integrating detector is proportional to the electrical and thus physical size of the integration capacitor, which is limited by the pixel's dimensions. For the chosen pitch of 110 µm this limits the dynamic range to ≈2.2 k photons at 12 keV. To cope with larger signals, shorter integration times or some form of charge removal is required. We plan to implement the latter in a 2$^{\text{nd}}$ generation of the readout ASIC.
The detector will provide a quasi dead-time free continuous operation at a frame rate of $f_{\text{FR}} \approx 150$ kHz, as illustrated in fig. 1. Thus 10 k photons at 12 keV translates to a maximum photon flux of ≈1.5 × 10^9 photons/pixel/s or ≈0.124 × 10^{12} photons/mm^2/s.

Figure 1: Principle of CoRDIA's continuous operation and signal path.

The Electron-collecting readout ASIC is also compatible with various sensors:
- Silicon - the sensor material suitable for the 4 . . . 15 keV range.
- High-Z materials - like Gallium Arsenide (GaAs), Cadmium Telluride (CdTe) or Cadmium Zinc Telluride (CZT). Sensors from these materials are still sensitive at energies ≫15 keV, and will be crucial to exploit the much higher flux of high energy photons at 4th generation sources.
- LGAD's - Low Gain Avalanche Diode sensors, featuring an internal gain and thus extending the sensitivity to energies ≪4 keV.

3 CoRDIA ASIC Architecture

The overall schematic of the CoRDIA ASIC is depicted in fig. 2, the circuits are described in the following.

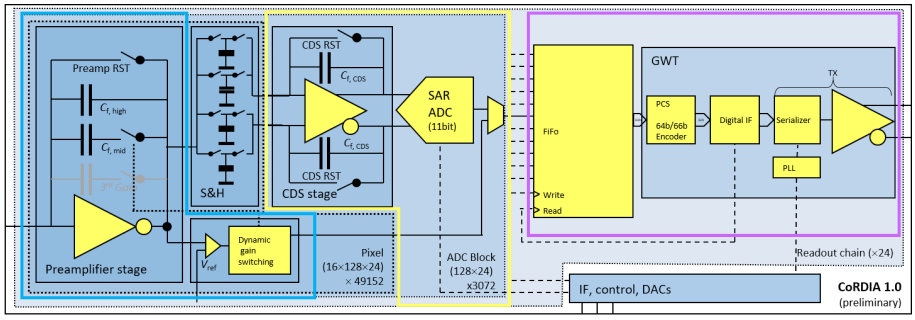

Figure 2: Block Schematic of the CoRDIA ASIC (assuming a chip size of 256 × 192 pixels).

3.1 Adaptive Gain Preamplifier

For the preamplifier we chose an implementation similar to the AGIPD [5] detector: A charge sensitive amplifier with adaptive gain switching, built around an inverter core. In adaptive gain mode, the preamplifier starts the integration of charges from the sensor on a tiny feedback capacitor, which yields a very high sensitivity and and a very low noise – lower than the Poissonian fluctuation of the measured signal itself. This way individual photons can be easily registered as in the left of fig. 3 shows. A discriminator at the preamplifier output can detect, if its amplitude reaches the end of the dynamic range, and if so a 2$^{\text{nd}}$, much larger capacitor is switched in parallel to the first: The collected charge redistributes on both capacitors and integration continues with a much lower slope, i.e. at much lower sensitivity. This is depicted on the right graph of fig. 3. Since the Poissonian fluctuation of a signal grows proportional to

[1] Continuous Wave

its square root, it remains still dominant compared to the increased preamplifier noise in the lower gain. After the acquisition of each image, the preamplifier is reset by discharging the feedback capacitors.

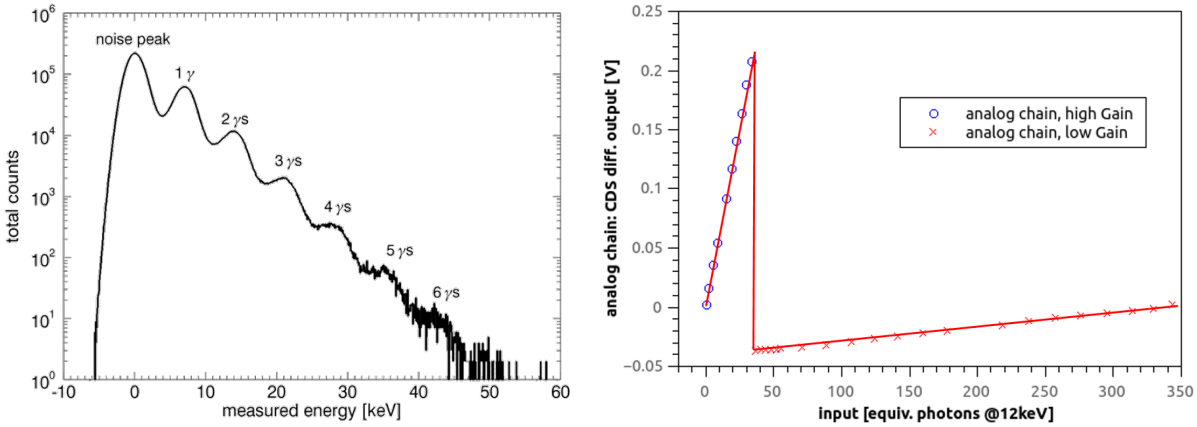

Figure 3: Left: Single photon sensitive integrating detector example (AGIPD).
Right: Adaptive gain characteristics of the CoRDIA 0.1 chip.

3.2 Correlated Double sampling Stage (CDS)

The output of the preamplifier is sampled twice per image by the subsequent sample-and-hold (S&H) stage: At the start and at the end of the integration. By evaluating the difference of these samples, reset noise and other fluctuations (e.g. of the preamplifier baseline) are removed and low frequency noise components are suppressed by the resulting bandwidth limitation. To achieve a dead time free operation, the S&H stage consists of four capacitors per pixel, two samples which are processed by the subsequent correlated double sampling stage (CDS), and two used for the acquisition of a new frame.
The CDS stage itself is a fully symmetric charge sensitive amplifier itself, built around a differential pair with common mode (CM) feedback. The choice of this architecture bears several advantages by providing the matching of the signals to the subsequent Analogue to Digital Converter (ADC): The CM feedback to the CM level of the ADC, a DC offset to the proper baseline and additional gain to match the ADC's dynamic range. Furthermore one CDS stage serves a block of 4×4 pixels, since the conversion rate of the subsequent ADC is about 16 times higher than CoRDIA's design frame rate of ≈150 kHz.

3.3 Analogue to Digital Converter

Digitisation of the image is done by an ADC using a differential charge division schema and the successive approximation register (SAR) approach. It converts 11 bit at 2.4 MS/s, reaching 10 ENOBs effective resolution.
The bits are converted sequentially, and a huge amount of buffering is avoided by transferring the output of 128 ADCs in parallel to the subsequent Gigabit Wire Transmitter.

3.4 Gigabit Wire Transmitter (GWT)

The GWT is based upon the same solution that is implemented on the Timepix 4 [9] chip. It implements an 64/66 bit encoded data stream consistent with the IEEE 802.3ae [10] standard, which allows the ASIC to interface with commercial hardware or FPGAs[2] – on board or via optical fibre links.
The GWT consists of several parts: First stage is a 128 bit wide FIFO to receive the payload data to be transmitted in an pixel-parallel (128 bit wide) form. Next is the *Physical Coding Sublayer* (PCS), mainly consisting of a polynomial scrambler, continuously fed with FIFO data, or an idle pattern, if the FIFO is empty. Two header bits are also generated, to identify the encoded data as payload or idle, increasing the data width to 66 bits. From these a *gearbox* generates 64 bit wide chunks at a higher rate to be sent to the transmitter part. For test purposes the PCS can provide square wave or PRBS[3] data. The actual circuit was synthesized from HDL[4] code provided by Nikhef.

[2]Field Programmable Gate Arrays [3]Pseudo Random Bit Sequence [4]Hardware Description Language

The PCS' output is serialised and driven off-chip by the transmitter (TX), provided by Nikhef as a full layout. Core component of this part is a multiplexer, driven by either of two DLLs[5]. For CoRDIA the slower one (at 5.12 Gbit/s) is used. The DLL's clock is provided by an on-chip PLL,[6] acting as a *clock cleaner* for utmost stability. The signals in the multiplexer and inverter based off-chip driver are fully differential for lowest possible BER[7] values.

4 CoRDIA ASIC Layout and Implementation

For the layout of larger chips, CoRDIA adopts *superpixels* – self-contained units of 16 preamplifiers together with S&H, and CDS stage, and an ADC. The footprint of such a *superpixel* is smaller than the 440 µm × 440 µm area of the sensor pixels. The pitch of the bump pads to these is adapted on the top metal layer. The remaining space is occupied by the channels for readout structures and those for power supply connections via TSVs[8] and slow control. The dimensions of the *superpixel* layout are such, that it fits the pitch of the digital standard cells of the chosen TSMC®[9] 65 nm CMOS process. This way automated tools can be used for layout generation and timing analysis of large chips. The concept of *superpixels* and the composition of larger layouts thereof is sketched in fig. 4.

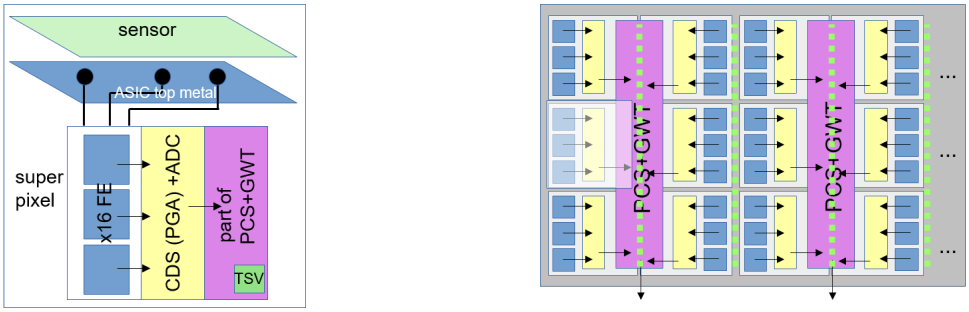

Figure 4: *Superpixel* structure (left) and sketch of a repetitive chip layout composed thereof (right).

5 CoRDIA Prototype ASICs

The circuit components described above have been individually manufactured and tested on four small ASICs manufactured on MPW[10] runs. The layouts of these are shown in fig. 6.

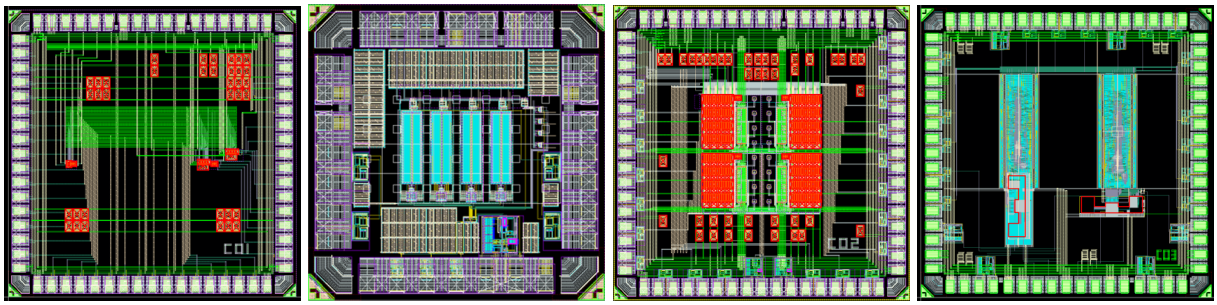

Figure 5: CoRDIA prototype ASICs from left to right: CoRDIA_01 implementing preamplifier and CDS stage, HSI_ADC01 with 4 flavours of SAR ADCs, CoRDIA_02 with four *superpixel* structures, CoRDIA_03 containing two GWT structures

CoRDIA_01 was taped out in 2021, and contains the preamplifier together with the S&H, and the CDS block. It was used to validate the expected frame rate, adaptive gain operation, and the continuous (integrate while reading out the previous sample) CDS operation.

[5]Delay Locked Loop [6]Phase Locked Loop [7]Bit Error Rate
[8]Through Silicon Via - electrical connection to the back side of the chip [9]Taiwan Semiconductor Manufacturing Company
[10]Multi project Wafer – Wafer with a reticle of multiple small designs

HSI_ADC01 contains four variants of an ADC based on the SAR architecture. It was used to select the optimal conversion depth, capacitor choice and switching options and proved image sapling at the desired rate. It was also taped out in 2021.
In 2023 *CoRDIA_02* was taped out, consisting of four *superpixel* layout blocks of 16 pixel frontends each, arranged in the final configuration, i.e. around the space later occupied by the GWT readout structure. It has been successfully tested, and characterised (as far as possible without mounting it to a sensor) using the Caribou [11] DAQ system. An example of signals injected in different patterns by the pulsed capacitor on-chip calibration source are shown in fig. 6.
CoRDIA_03 was submitted to explore and validate the PCS and GWT circuit. Taped out in 2024, the CoRDIA_03 prototype implements two variants of these, optimised for the data flow and layout requirements on CoRDIA. It is currently being tested using the Caribou system, and also first results are available, as fig. 6 shows.

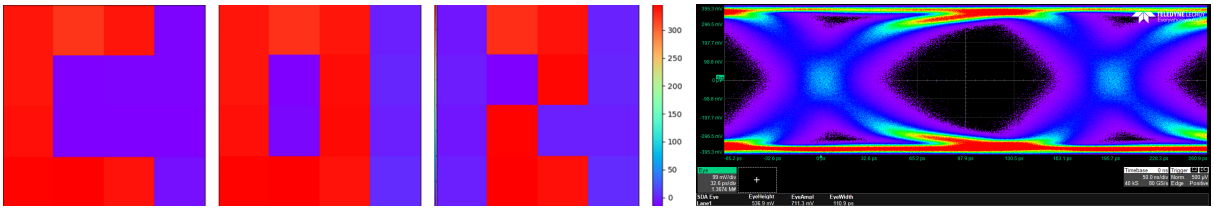

Figure 6: Left: CORDIA_02: Pattern of pixels with signals injected by the on-chip calibration circuit. Right: CORDIA_03: Eye Diagram of the GWT sending a PRBS31 pattern at at 5.12Gb/s.

6 Towards a CoRDIA Detector System

On the system level, CoRDIA aims to overcome some of the shortcomings and disadvantages of the present detector systems like [3, 4, 5]. In particular we aim at the following improvements:
Gapless Modules: By using TSVs to connect the readout ASICs, the size of a detector module can be shrunk to the area of the sensor, without any gap between modules required e.g. by the wire bonds connecting the ASICs. With the development of *edgeless sensors* the only remaining insensitive area, i.e. that of guardring structures on the sensor itself, could also be removed.
Simple Modules: A detector module of a hybrid pixel detector usually consists of two parts: A *hybrid* carrying sensor and ASICs, and a *readout board* (RoB), providing power and control signals to the ASICs and processing the data and formatting it to some commercial standard. For CoRDIA the 2nd task can be omitted, since the IEEE 802.3ae compatible 64/66 bit encoding of the readout data enables the use of commercial optical links (e.g. SAMTEC® Firefly) and direct connections to commercial hardware or FPGAs. Thus the RoB only needs to provide power and control signals to the ASICs and host optical transmitters to send the data to the commercial hardware (e.g. ALVEO® or µTCA FPGA cards) of the next stage.
Data Reduction: A 1 Megapixel detector with a resolution of 12 bit/pixel at 150 kHz produces a data volume of

$$1\,048\,576\,\text{pixel} \times \frac{12\,\text{bit/pixel}}{8\,\text{bit/Byte}} \times 150\,\text{kHz} = 235.9\,\text{GByte/s},$$

which means it literally fills a hard disk every 4 seconds. Such huge data volumes can neither be sustainably stored, nor efficiently analysed and data reduction becomes a severe must.
However, the appropriate method to perform data reduction is considered to be strongly dependent on the type of experiment performed, as the following list explains:

- *Event Selection* is an appropriate method to get rid of poor images, e.g. if in single molecule imaging and liquid or gaseous jet experiments no sample is hit.
- *Zero Suppression* can be appropriate for diffraction images of any kind of weakly scattering samples.
- *Cluster Finding* can e.g reconstruct *Bragg Peaks* on the fly.
- *Lossless or Lossy Compression* are more universal methods of data reduction.
- *Experiment specific algorithms* e.g. to calculate correlation functions in XPCS[11] experiments.

This fits very well together with the use of powerful commercial FPGA cards as the first DAQ stage, on which after applying calibration the data reduction or reconstruction algorithm matching the type of experiment is executed. Fig. 7 illustrates the advantages of CoRDIA's concept over present systems.

[11] X-ray Photon Correlation Spectroscopy

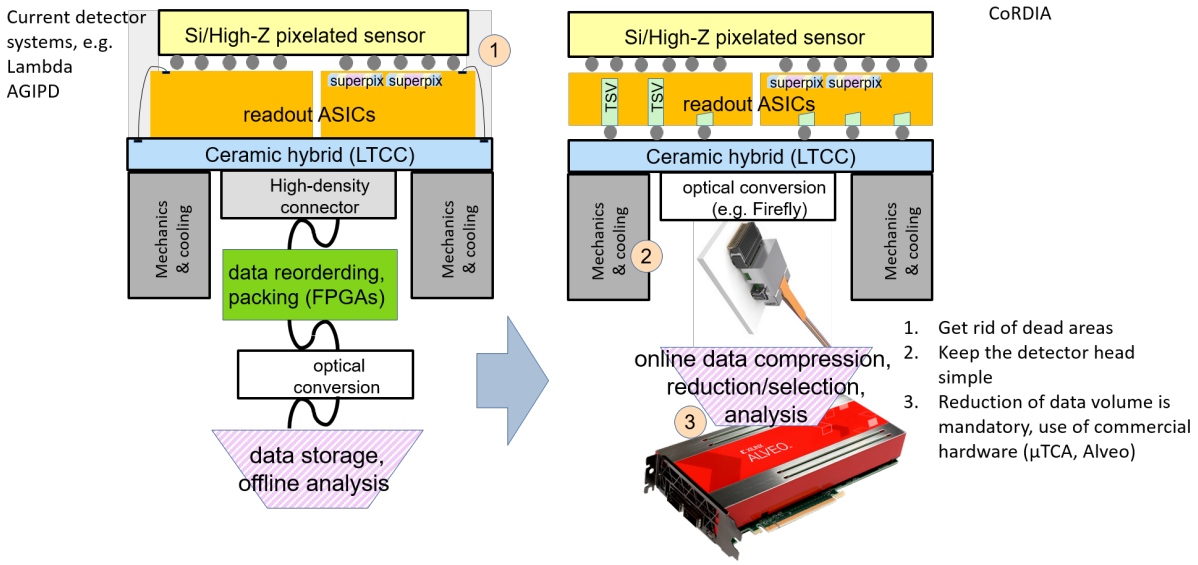

Figure 7: Sketch of the improvements of a CoRDIA system over contemporary hybrid pixel detectors.

7 Next Steps and Conclusions

The next, i.e. CoDIA_04 ASIC prototype will integrate the full signal chain for $128 \times 16 = 2048$ pixels. This prototype will have a compact pixel matrix, such that it can be mounted to a sensor. The channel with the readout circuitry will therefore not be straight as expected on a full-scale chip, but has to meander through the matrix of *superpixels*.

CoRDIA_10 will then be a the full-scale (most probable 256×192 pixel) chip, from which we intend to produce detector modules and to integrate it with commercial DAQ hardware to arrive to scalable detector systems before the start of PETRA IV, expected in 2032.

Along with the hardware development we plan to implement calibration algorithms and a basic set of data reduction methods to counter the '*Data Deluge*' expected with 4$^{\text{th}}$ generation sources.

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