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4D-tracking with digital SiPMs

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ABSTRACT

Silicon Photomultipliers (SiPMs) are the state-of-the-art technology in single-photon detection with solid-state detectors. Single Photon Avalanche Diodes (SPADs), the key element of SiPMs, can now be manufactured in CMOS processes, facilitating the integration of a SPAD array into custom monolithic ASICs. This allows implementing features such as signal digitization, masking, full hit-map readout, noise suppression, and photon counting in a monolithic CMOS chip. The complexity of the off-chip readout chain is thereby reduced.

These new features allow new applications for digital SiPMs, such as 4D-tracking of charged particles, where spatial resolutions of the order of 10 μm and timestamping with time resolutions of a few tens of ps are required.

A prototype of a digital SiPM was designed at DESY using the LFoundry 150 nm CMOS technology. Various studies were carried out in the laboratory and at the DESY II test-beam facility to evaluate the sensor performance in Minimum Ionizing Particles (MIPs) detection. The direct detection of charged particles was investigated for bare prototypes and assemblies coupling dSiPMs and thin LYSO crystals. Spatial resolution $\sim 20 \mu\text{m}$ and a full-system time resolution of $\sim 50 \text{ps}$ are measured using bare dSiPMs in direct MIP detection. Efficiency $>99.5\%$, low noise rate and time resolution $<1 \text{ns}$ can be reached with the thin radiator coupling.

1. Introduction

Silicon Photomultipliers (SiPMs) represent a solid-state version of conventional photomultipliers (PMTs). SiPMs are arrays of Single Photon Avalanche Diodes (SPADs) read out in parallel. SiPMs produce a signal approximately proportional to the number of incident photons, which is then processed with dedicated electronics. SiPMs are operated at relatively low voltages, have high gain, good photon sensitivity, excellent intrinsic timing, and are insensitive to magnetic fields. These characteristics fulfil the requirements of most High Energy Physics (HEP) photodetectors [1].

Some commercial CMOS foundries have introduced SPAD diodes in their Process Design Kits (PDKs). It is therefore possible to design digital SiPM integrated circuits (dSiPM from now on) where CMOS electronics and avalanche diodes are on the same silicon die. Signal digitization can take place at the level of individual SPADs. Customized circuits and readout architectures can be implemented, simplifying the DAQ system and reducing the system power consumption. Low-cost implementation

of custom designs and large-volume production are further advantages offered by CMOS foundries. The main drawbacks of CMOS dSiPMs are the smaller fill factor and higher Dark Count Rate (DCR) compared to conventional SiPMs [2].

CMOS SPADs development is mainly driven by commercial applications such as Light Detection and Ranging (LIDAR) systems and 3D-Imaging [3]. However, the properties of these sensors make them excellent candidates in new HEP applications such as scintillating fibres readout [4] or 4D-tracking of Minimum Ionizing Particles (MIPs), which is the main topic of this work.

The possibility of direct detection of MIPs with SPADs and SiPMs has already been proven [5,6]. Due to the large number of electron-hole pairs created by an impinging MIP, an avalanche is triggered, with a high probability, and within few 10ps, as soon as a SPAD is hit. Through the integration in a CMOS circuit, it is possible to develop chip readout architectures typical of tracking detectors with SPADs as MIP-sensitive pixels.

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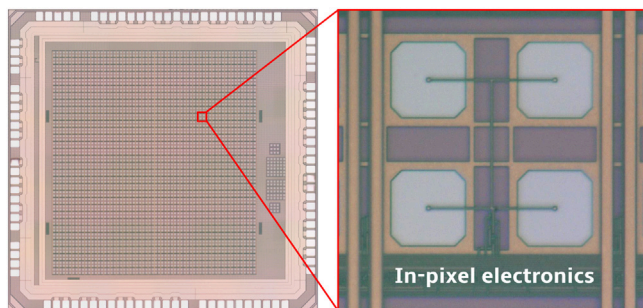


Fig. 1. Microscope picture of the DESY dSiPM chip (left). A magnified version of a pixel made of four SPADs sharing in-pixel electronics (right).

2. DESY dSiPM prototype in CMOS 150 nm technology

A prototype of dSiPM was designed at DESY using a LFoundry 150 nm CMOS technology [7]. The chip includes pre-defined SPAD layout provided by the company and CMOS electronics. The main array includes 32×32 pixels and has a total area of $\sim 2.2 \times \sim 2.4 \text{ mm}^2$. Each pixel contains four SPADs connected in parallel that share the same in-pixel electronics. Fig. 1 shows a microscope picture of a diced chip (left) and a zoom into a single pixel (right). The total pixel size is $69.6 \times 76 \mu\text{m}^2$. The four SPADs of the pixel have a nominal active area of $20 \times 20 \mu\text{m}^2$ (white regions in Fig. 1 right), the remaining area of the pixel is occupied by trenches and electronics well. This results in an effective fill factor of the pixel (i.e. of the sensor) of 30%. In-pixel electronics include a globally biased quenching transistor and a masking circuit. An inverter for signal digitization and a 2-bit hit counter are also part of the in-pixel circuit. In the chip periphery, four shared Time-to-Digital Converters (TDCs) allow time-stamping with $\sim 95 \text{ ps}$ bins. The full hit-map can be read out and validation logic is implemented for event discrimination.

All chip characterizations were performed using the versatile Caribou DAQ system [8]. It provides all bias and reference currents/voltages as well as clocks required for chip operations. The system is also used for chip configuration and data readout thanks to high-speed LVDS links and the system-embedded FPGA. The readout is frame-based and operates at 3 MHz frame rate. More details on the sensor design and the DAQ system, together with chip characterizations can be found in [7].

3. Test-beam characterization of DESY dSiPM

In order to evaluate sensor performances in 4D-tracking of MIPs, several test-beam experiments were carried out on prototypes. Two main configurations have been investigated: bare silicon (Section 4) and dSiPMs coupled with thin radiators (Sections 5 and 6).

Test-beam studies took place at the DESY II test-beam facility [9]. The facility provides electron beams in the energy range 1 to 6 GeV as well as reference beam telescopes for precise tracking [10,11]. An AIDA Trigger Logic Unit (TLU) [12] and the EUDAQ framework [13] were employed for devices synchronization and data acquisition. A fast scintillator was used to get a region of interest trigger and another scintillator with a hole as a veto. Active cooling allowed for stable operations at different temperatures down to 0°C . The precise temperature of the dSiPM was monitored using a temperature diode implemented in the chip periphery.

Fig. 2 shows the test-beam setup, a schematic sketch is shown in [14], Figure 3. Two mechanically aligned Devices Under Test (DUTs) were investigated simultaneously to allow timing studies using time differences. Details of the setup and measurement campaigns can be found in [14].

Test-beam data analysis was performed using the Corryvreckan framework [15].

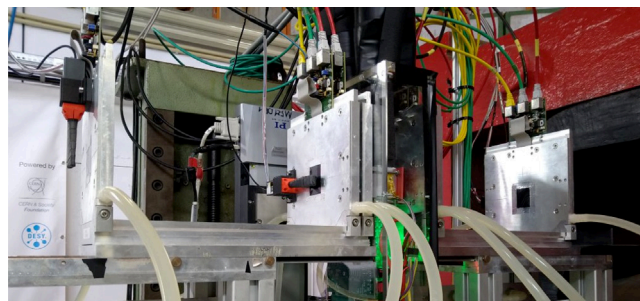


Fig. 2. Test-beam setup in the DESY II facility using EUDET type telescopes as reference for track reconstruction and two cooled DUTs in the middle.

4. Performance of bare dSiPM

In the first test-beam campaigns bare dSiPMs were exposed to the electron beam to evaluate their spatial and temporal performance in direct MIP detection. The main results of these measurements are reported in [14] and the data analysis of further investigations is ongoing.

The cluster size of MIP events on bare dSiPM associated with reconstructed tracks is mainly one (see Fig. 3 left). The cluster size is expressed in pixel units as the pixel readout structure does not provide information on the number of in-pixel firing SPADs. Cluster size larger than one is observed in a small percentage of the events and is consistent with the intrinsic crosstalk of SPADs. This means that noise hits cannot be distinguished from MIPs, only based on event topology. In the test-beam environment though, the precise telescope tracking results in a few micrometre track position resolution at the DUT level allowing for the correct association of signal events with the corresponding track.

In [14] spatial resolution in MIP detection is estimated from spatial residuals to be of the order of $20 \mu\text{m}$ and efficiency is measured to be of the order of 32%. This value is comparable with the nominal fill factor of dSiPM. An in-pixel efficiency map can be obtained by projecting the particle intercepts with the DUT into a single pixel and averaging the efficiency for the binned in-pixel positions. Fig. 4 (left) from [14] shows an example of bare dSiPM in-pixel efficiency map. It can be noted that the pixel is efficient at SPADs and inefficient in the in-between area due to SPAD trenches and in-pixel electronics.

The temporal resolution of the bare dSiPM in MIP detection is also investigated as described in [16]. In the reference the time residuals are obtained by subtracting the timestamps of coincident MIP events in the two aligned DUTs. A temporal resolution of $45 \pm 6 \text{ ps}$ is measured in about 85% of the associated events. A slower component in nanosecond regime characterizes the remaining fraction of the data. This is due to MIP interactions in SPAD edge regions in one of the two DUTs. It should be emphasized that the timing performance reported here includes all contributions from the entire dSiPM DAQ system.

5. The thin radiator concept

One of the main drawbacks in direct MIP detection using bare dSiPMs is the limited efficiency due to the low fill factor. An inactive region between SPADs is needed to contain the avalanche within a single SPAD and additional space is used to host the in-pixel CMOS electronics. To overcome this limit a thin radiator coupled to the dSiPM can enhance the efficiency with a tolerable decrease of the spatial resolution.

In [6] it was shown that using SiPM in direct MIP detection the resin employed to protect the sensor produces Cherenkov light. This

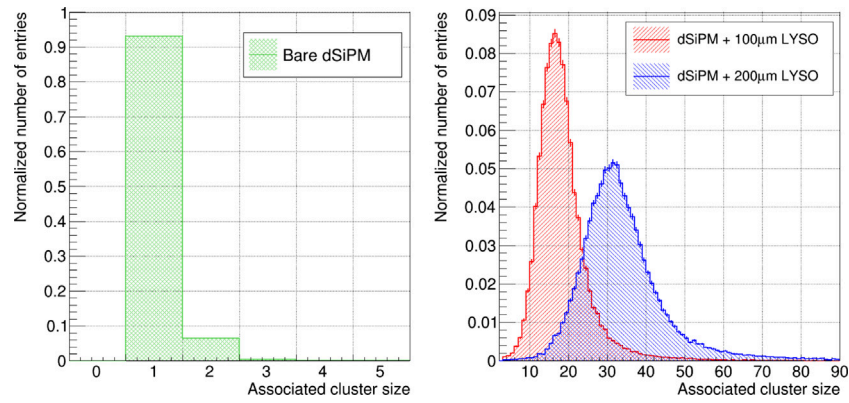


Fig. 3. Normalized associated cluster size of MIP events in test-beam for bare dSiPM (green), dSiPM+100µm LYSO (red) and dSiPM+200µm LYSO (blue). Plots refer to dSiPMs operated at 0°C and 2 V overvoltage.

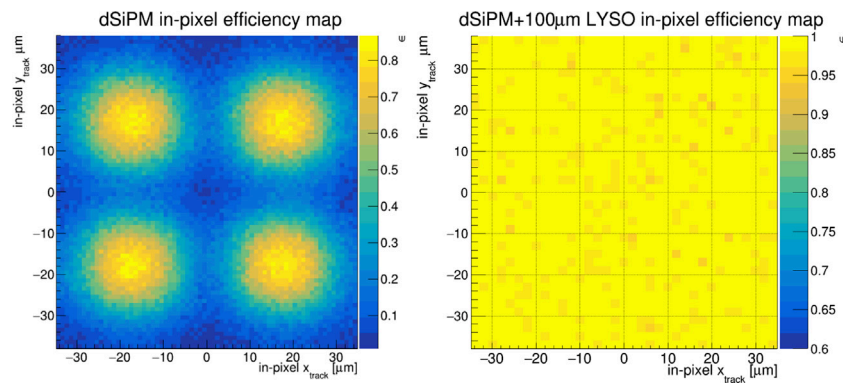


Fig. 4. In-pixel efficiency map in MIP detection for bare SiPM from [14] (left) and for dSiPM+100µm LYSO (right). In the reported example, the samples are operated at 0°C and 2 V overvoltage.

improves the sensor efficiency and creates multi-SPAD signals. Following the same concept, scintillators with thicknesses of the O(100µm) and high light yield can be coupled to the dSiPM. A MIP crossing the radiator releases energy and scintillation light is produced along its path. The light is isotropically emitted but due to the reduced thickness of the radiator is mostly confined and detected in a region close to the original MIP interaction point.

To test this concept, LYSOs with sizes of $\sim 2.5 \times \sim 2.5 \text{ mm}^2$ and thicknesses in the range 100µm to 1 mm were produced by OST Photonics company with the two large faces polished. The crystals are coupled to dSiPM prototypes using Polytec EP 601-LV epoxy adhesive. Fig. 5 shows two dSiPM samples coupled with 100µm (left) and 200µm (right) thick crystals.

After crystal coupling, the samples were tested using a Sr-90 source. Fig. 6 shows an example of a hit map obtained with a Sr-90 source for the two assemblies in Fig. 5. It can be noted that most of the hits are confined to clusters as expected. Only touching pixels are considered part of the cluster. The cluster centre is defined as the average position of pixels in the cluster. The original particle position can then be estimated as the cluster centre.

6. Performance of dSiPM with thin radiator

Further test-beam campaigns were carried out on the prototypes coupled with thin radiators to evaluate the 4D-tracking performance.

The first major difference in MIP detection with thin LYSOs coupling can be seen in the associated cluster size. Fig. 3 shows the normalized cluster size of MIPs events for bare dSiPM, dSiPM+100µm LYSO and dSiPM+200µm LYSO. The comparison is made between runs where the

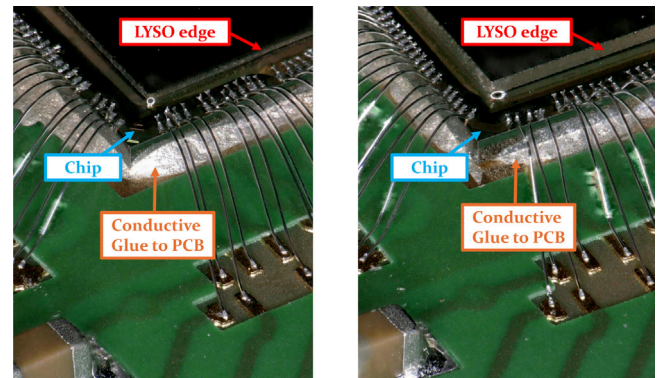


Fig. 5. Thin LYSO crystals glued on dSiPM samples. 100µm (left) and 200µm (right) thick LYSOs coupling is shown.

chips were operated at the same temperature and overvoltage. The bare silicon events have a cluster size that is mainly one. With the thin LYSO crystals, the cluster size increases considerably due to scintillation photons. This way, MIP events can be clearly distinguished from noise events. Noise signals involve dominantly one or two pixels (if crosstalk happens) and therefore have small cluster sizes (comparable with the bare dSiPM case). For geometrical reasons, the cluster size increases with the thickness of the radiator.

The spatial resolution of the dSiPM+LYSOs prototypes was evaluated by analysing at the spatial residuals between the track intercept

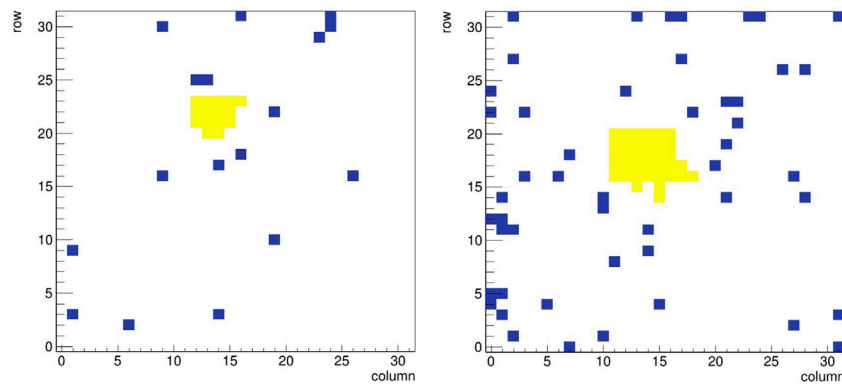


Fig. 6. Hit maps obtained with a Sr-90 source of dSiPM coupled with 100 μm LYSO (left) and 200 μm LYSO (right). Reconstructed clusters are marked in yellow. Chip operated at room temperature with 2 V overvoltage.

Table 1

DESY dSiPM 4D-tracking performance in MIP detection. Bare dSiPM (first column) and dSiPM with thin LYSO coupling (second column).

	dSiPM	dSiPM + LYSOs
MIP cluster size	~ 1 pixel	$\sim 20\text{--}40$ pixels
Spatial resolution	~ 20 μm	$\sim 32\text{--}38$ μm
Efficiency	$\sim 32\%$	$>99.5\%$
Time resolution	50 ps ^a	<1 ns ^b

^a In the SPAD active area.

^b Work in progress.

with the DUT and the reconstructed cluster centre. The spatial resolution, defined as the sigma of the Gaussian fit on the spatial residuals, is ~ 32 μm for the 100 μm LYSO sample and ~ 38 μm for the 200 μm LYSO sample.

The MIP detection efficiency of dSiPMs coupled with thin LYSOs is defined as the ratio between the tracks intersecting the DUT and the subset of tracks with an associated cluster on the DUT. A spatial cut of 200 μm and a time cut of 2 μs is applied in cluster association for this measurement. Efficiency is measured to be $>99.5\%$ for all the tested overvoltages and temperatures. An example of an in-pixel efficiency map is shown in Fig. 4 (right). Here the pixel is fully efficient with no dead regions contrary to what is presented in Fig. 4 (left) for the bare dSiPM case, where only $\sim 32\%$ of the pixel is efficient.

The temporal resolution of dSiPM+LYSOs is currently being investigated. Preliminary results show a time resolution in the nanosecond regime when the MIPs do not hit a SPAD directly. In this scenario timing response is assumed to be dominated by the scintillation process. Faster or higher light-yield scintillators could result in better timing.

7. Conclusion & outlook

Digital SiPM integrated circuits represent an interesting technology for future detector systems in HEP and beyond. Low power budget, on-chip digitization and data processing, excellent granularity, fast timing, large volume and low-cost production are some of the potential advantages offered by CMOS dSiPMs.

As a possible application of the technology, MIPs 4D-tracking is studied. The sensor was successfully integrated into a test-beam setup and operated as a particle detector. DESY dSiPM prototype was tested as bare silicon and coupled with thin LYSO crystals. The spatial and timing performance of the prototypes were investigated. The main results of the measurements are summarized in Table 1.

The proof of concept of the thin radiator coupling was successful, demonstrating full efficiency, good spatial resolution, and low noise rates. Further investigations will determine whether the technology can meet all 4D-Tracking requirements. In particular, the use of faster radiators or higher-performance SPADs in different CMOS process nodes could allow high-demanding timing performance to be met.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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