Development of the Readout Electronics for a MAPS-Based Beam Telescope

Yao Teng, Changqing Feng, Yi Liu, Chenfei Yang, and Shubin Liu

***Abstract*— Along with the change of the Deutsches Elektronen-Synchrotron (DESY) II test beam facility operation mode, the existing beam telescope built with the Mimosa26 chips will be unable to meet the requirements of the much-increased beam particle rate. In this article, we present the readout electronics of a new beam telescope built with ALice PIxel Detector (ALPIDE) chips which are originally designed for the upgrade of A Large Ion Collider Experiment (ALICE). The gigabit Ethernet implemented in the high-speed transceiver of Kintex field programmable gate array (FPGA) enables individual data acquisition and control of each ALPIDE chip. The data from the multidetector plane are transmitted to the remote platform via an Ethernet switch. The global trigger is generated by an AIDA2020-trigger logic unit (TLU) by the coincidence of two pairs of plastic scintillators. The results of long-term beam tests show that the new beam telescope can achieve a lower fake hit rate and a trigger rate of 220 kHz, which increases beam utilization and reduces the difficulty of track reconstruction. The biased resolution of distribution using all six planes for tracking in a 6 GeV electron beam is measured to be about 5 μm.**

***Index Terms*— ALice PIxel Detector (ALPIDE), beam telescope, monolithic active pixel sensor (MAPS).**

I. Introduction

THE beam telescopes are high-precision apparatuses that are used to reconstruct the track of the particles [1]. A typical beam telescope has multiple layers of position-sensitive detectors. In a beam experiment, the detector under test (DUT) is installed in the middle of the multilayer beam telescope system. The position resolution and other properties of the DUT can be measured based on the hits of the particle on the DUT and each detector plane of the beam telescope. One example of the beam telescope is the widely used EUDET [2]-style beam telescope at Deutsches Elektronen-Synchrotron (DESY) test beam facility [3], [4], [5].

DESY has its own electron synchrotron called DESY II, which has a circumference of 292.8 m. The energy of the particles in the ring oscillates in a sinusoidal mode between 456 MeV and 6.3 GeV [6]. The generation of the test beam is illustrated in Fig. 1 [6].

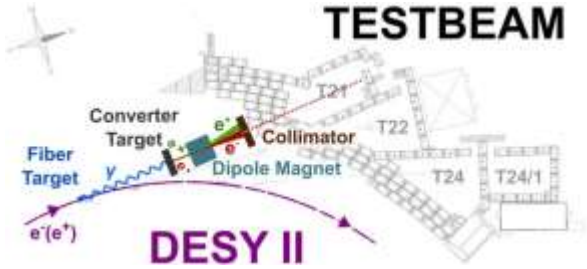

Fig. 1. Schematic of a test beam at DESY. One 25 μm thick fiber target is placed in the main ring of the DESY II, and the electron bunch collides with it to generate bremsstrahlung radiation. The resulting γ -photons hit the converter target and generate electron–positron pairs, which are then screened by a dipole magnet and collimator and finally enter the experimental beam area, which can be accessed by the users when the installed beam shutter is off. By adjusting the current of the dipole magnet, i.e., modifying the magnetic field strength, the energy of the experimental beam particles that eventually pass through the collimator can be adjusted.

There are three test beam lines that provide users with EUDET-style beam telescopes at the DESY test beam facility. These beam telescopes were built with the Mimosa26 sensor chips and they have been undergoing a continuous upgrade for nearly a decade. Benefiting from the excellent spatial resolution of Mimosa26 [5], [7] sensor chip and its low material budget, the EUDET-style beam telescopes can reach a distribution resolution of 1.83 μm [8] for a 6 GeV electron or positron beam on the DUT. This is sufficient for most test beam experiments for detector prototypes.

There is a plan to update the beam lines on the DESY test beam facility by changing their operation mode, which could provide a beam particle rate up to 100 kHz [6]. The EUDET-style beam telescopes fail to meet the requirements of the upgraded beam lines because of their low trigger rate as the readout time per frame is about 112.5 μs [8]. Therefore, a new beam telescope has been developed. In this article, the readout electronics architecture of the new telescope is described and its performance based on beam tests is presented.

II. Requirements for Telescope System Design

The low trigger rate became the key limitation of the current Mimosa26-based EUDET-style beam telescope. The low maximum trigger rate is due to the rolling shutter mode. The readout frequency of Mimosa26 chip is about 10 k frames/s [5].

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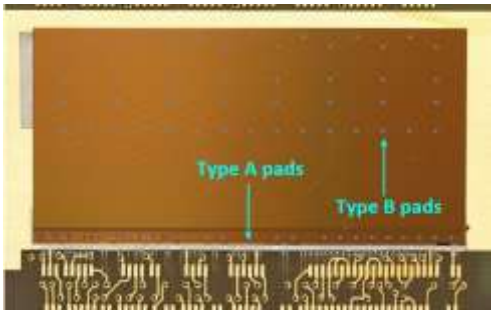

Fig. 2. Photograph of the ALPIDE chip. The rectangular part with metallic shine in the picture is the front side of the chip. The rounded edge with a diameter of 290 μm is the opening in the passivation layer of the type B pads. The type A pads are located under the chip. This figure is shown that the ALPIDE chip is bonded through type A pads.

The Mimosa26 chip has about 40 fake hits per readout frame [8], which is even higher due to the aging of the Mimosa26 chip. The high fake hit rate level results in an increased amount of data and compromised tracking performance. In addition, the production of Mimosa26 chips has been ended, which is a major challenge for the current beam telescope maintenance. Therefore, a new silicon pixel beam telescope system is in urgent need.

In this study, a new monolithic active pixel sensor (MAPS) chip called ALice PIxel Detector (ALPIDE) was adopted to replace the Mimosa26 for the new EUDET-style beam telescopes. The readout electronics also had to be redesigned. A photograph of the ALPIDE chip is shown in Fig. 2 [9], [10].

The readout mode of the ALPIDE chip is the global shutter, i.e., all pixels of the whole matrix are shaped and over-threshold screened at the same time, and the hit signal latching is completed upon the arrival of a global trigger signal. Every two columns of pixel points share one set of front-end readout circuits. The circuit transmits the latching data to the periphery circuit at the bottom of the chip by priority encoder and in-matrix zero suppression. Such encoding methods greatly reduce dead time. The low-voltage differential signaling (LVDS) high-speed serial data link which can reach a speed up to 1.2 Gb/s allows fast readout.

To ensure that the existing test beam users can seamlessly migrate to the new beam telescope platform, the new beam telescope should be fully compatible with the old trigger logic unit (TLU) interface and the current data processing system called EUDAQ2 [11].

In summary, the next generation of beam telescope electronics needs to meet the following requirements.

1) A trigger rate up to 100 kHz.
2) A noise level well below that of the original beam telescope for more efficient utilization of the beam and a cleaner tracking environment.
3) Resolution of distribution at the order of micrometers (around 5 μm at 6 GeV).
4) High-speed electronics for the ALPIDE chips.
5) Fully compatible with the interface of TLU and EUDAQ2.

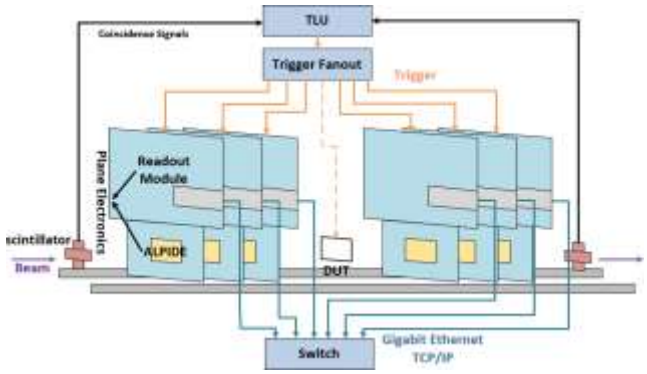

Fig. 3. Design of the ALPIDE beam telescope system. There are two pairs of plastic scintillators placed crosswise on both sides generating pulses when they are hit by the electron beam. The coincidence signal of these pulses is considered the global trigger. The trigger signal is generated after the TLU processed the global trigger. The trigger fan-out boards fan-out the trigger signal to each telescope plane as well as the DUT. The telescope planes and the DUT are mounted on a slide rail. The plane electronics consist of a readout module and the ALPIDE chip. There is a switch connecting all the planes.

III. Electronics of the Beam Telescope

A. Introduction of the ALPIDE Chip

The ALPIDE sensor chip manufactured in Towerjazz 0.18μm CMOS process [12] is designed for the inner tracker upgrade project of A Large Ion Collider Experiment (ALICE) at CERN. It consists of a total of 512 rows $\times$ 1024 columns of pixels with a sensitive area of 30 $\times$ 13.8 mm [13]. The in-pixel circuit of the ALPIDE pixel has more functions than that of Mimosa26. Therefore, its pixel pitch, 29.24 $\times$ 26.88 μm, is about 1.5 times of Mimosa26 pixel pitch. The power density of ALPIDE chip is reported to be lower than 40 mW/cm^2 [9], which is much lower than 250 mW/cm^2 of the Mimosa26 chip [5]. Since the pixel of ALPIDE can be individually masked, the number of fake hits is significantly reduced [11].

The excellent performance of the ALPIDE sensor chip makes it a great detector sensor for the next generation of beam telescopes.

B. Architecture of the ALPIDE Beam Telescope

The ALPIDE beam telescope system is built with six telescope planes, as shown in Fig. 3. The planes are mounted on a moving platform on an aluminum slide rail, which is the same as the EUDET-style telescope, and the space among the planes can be freely adjusted. The planes are often divided into two equal groups called arms, which are mounted in the front and end, respectively. The DUT can be mounted between the two arms with a moving platform to facilitate adjustment of the position of the detector.

Accidental collision, vibration, and dust can damage the chip during its long-term operation. In addition, the performance degradation of ALPIDE due to excessive radiation is not negligible. Therefore, the electronics are designed into two parts. The front-end board is bonded to the ALPIDE, which carries a small number of chips in addition to ALPIDE to reduce the replacement cost. The readout module implements the functions of data acquisition and control management. In this study, the front-end board is called the carrier board,

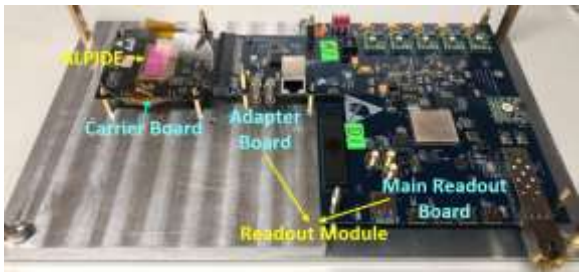

Fig. 4. Photograph of the electronics of a single telescope plane. A readout module consists of a main readout board and an adapter board. The ALPIDE sensor chip is bonded to the carrier board.

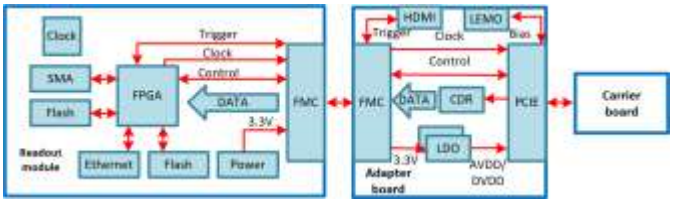

Fig. 5. Block diagram of the telescope plane electronics. This block diagram illustrates the data acquisition, slow control, clock supply, and power supply for the ALPIDE carrier.

and the readout module consists of a main readout board and an adapter board. A photograph of the electronics of a single plane is shown in Fig. 4.

An AIDA2020-TLU [14] generates the global trigger by the coincidence of two pairs of plastic scintillators placed crosswise on both sides. The trigger along with the trigger identification (ID) is sent to each electronics module and DUT. The AIDA2020-TLU is illustrated as TLU in Fig. 3.

There could be some distance between the test beam hall and its control room. In the meantime, each telescope plane with its electronics requires a data link and a control link to the remote room. The gigabit Ethernet based on TCP/IP protocol is used. All of the control links and data links run on the Ethernet network. It allows the software on the remote computer to manage the hardware electronics.

C. Design of Plane Electronics

The electronics of a single telescope plane is separated into three boards: carrier board, adapter board, and main readout board, as shown in Fig. 4. The carrier board is bonded to the ALPIDE sensor chip. The adapter board connects with the carrier board and the main readout board. The main readout board is used to collect the data from the carrier board and complete the communication with the computer. The block diagram of the overall architecture is shown in Fig. 5. The power supply in the caption of the Fig. 5 includes analog drain power voltage (AVDD) and digital drain power voltage (DVDD) [11].

1) Carrier Board: The carrier board provided by the ALICE experiment with the ALPIDE sensor chip bonded to it is used for the electronics design, as shown in Fig. 6. It allows for simplifying the maintenance of the beam telescope by easily replacing the sensor chip in case of sensor damage.

There are two data transfer ports on the PCIe connector: the 8-bit parallel data port and the LVDS high-speed serial

Fig. 6. Photograph of the carrier board (front view).

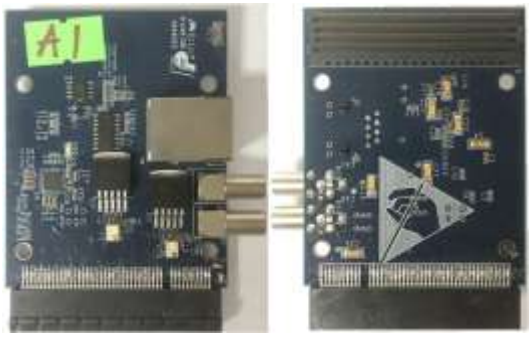

Fig. 7. Photograph of the front and back of the adapter board.

data port. As an additional note, the carrier board does not use the protocols and pin definitions of the PCIe specification. The 8-bit parallel data port is CMOS bidirectional data port intended to implement a shared parallel data bus between the outer barrel module slave chips and the associated master. The LVDS high-speed serial data port is used for the high-speed serial transmission of data between chips and the off-detector electronics. It is used by chips configured as inner barrel chips or outer barrel module master [11]. In this study, the serial data port is required.

The control pins of ALPIDE include a pair of Differential bidirectional ConTRoL ports (DCTRL). The DCTRL pins are bonded to the PCIe connector through the peripheral circuit. The DCTRL pin enables functions such as reset, pulse, and register reading and writing.

2) Adapter Board: The block diagram of the adapter board is shown in Fig. 5 and a photograph of the adapter board is shown in Fig. 7. The main purpose of the adapter board is to connect the main readout board with the carrier board. A male FPGA Mezzanine Card (FMC) header on one end for plugging in the main readout board, and a PCIe female connector on the other end for plugging in the carrier board.

The serial data interface of ALPIDE sensor chip for data readout is configured on its speed mode at 400 Mb/s. The adapter board is designed with a clock data recovery (CDR) chip. The clock and data recovered by the CDR chip are LVDS differential signals, which are connected to the field programmable gate array (FPGA) of the data interface board through the FMC connector. In addition, the trigger signal is transferred to the main readout board via the adapter board.

Fig. 8. Photograph of the main readout board. A: FPGA; B: Gigabit Ethernet connector; C: USB3.0 PHY chip; D: USB type-A female connector; E: JTAG-SMT module; F: FMC female connectors; and G: power supply modules.

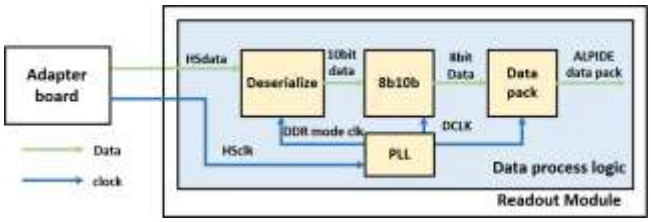

Fig. 9. Schematic of the data packing process within the FPGA. The data need to be deserialized and 8b/10b decoded before being packaged.

3) Main Readout Board: The main readout board which carries the FPGA is shown in Fig. 8. The main readout board acquires data measured by ALPIDE sensor chip on the carrier board. It also performs preliminary processing and packaging of the data before sending them on the Ethernet network. It receives the user operation commands from the software on the remote computer via the network and forward them to the carrier board according to the control protocol of the ALPIDE chip sensor.

As mentioned above, high-speed serial data at 400 Mbit/s from the sensor chip needs to be read out. In this project, a CDR chip is used to recover the clock domain from the data inputs. The final signals are then processed by FPGA.

Fig. 9 shows the processing of ALPIDE data inside the FPGA. After receiving the trigger pulse, the ALPIDE sensor chip starts to transmit the hit information of the latest measurement time window which is a readout frame. The high-speed serial data needs to be deserialized and then 8b/10b decoded to get the preliminary information. The hit information is retained on demand and combined with the trigger ID from the AIDA2020-TLU. Each readout frame is packaged into a separate packet and queued in the first in first out (FIFO) waiting to be sent.

Considering that the maximum effective data rate of the ALPIDE chip is 320 Mb/s in the outer bucket operation mode, a high-speed and stable data transmission channel is also required between the main readout board and the computer. To achieve a more flexible system architecture and stable long-distance data transmission, a gigabit Ethernet data transmission solution is used in the beam test. The data interface

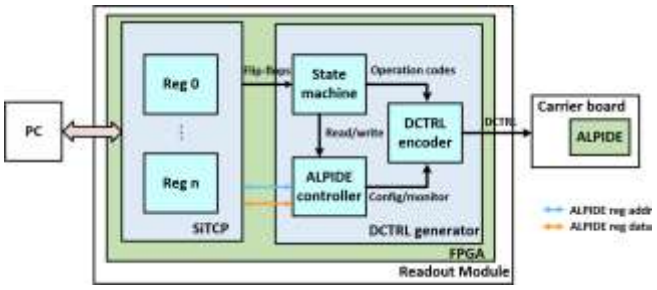

Fig. 10. Logic block diagram of ALPIDE slow control. The control signals of the ALPIDE chip are opcodes and read/written to the internal registers. The control of these two types is implemented in hardware in different ways. The software on the remote computer reads and writes the registers inside of the SiTCP implement. There are two groups of registers. The state machine composes one set of registers into the corresponding opcodes. Another set of registers stores the information of the ALPIDE configuration information. The opcodes and ALPIDE configuration information are encoded as differential serial signals. The differential signal enables the slow control of the ALPIDE through the DCTRL pins.

board is also designed with a USB 3.0 module to facilitate laboratory testing.

The logical block diagram of slow control is shown in Fig. 10. The software on the remote computer reads and writes the registers inside of the SiTCP implement. There are two groups of registers. One group keeps the states and the other has the configuration information of ALPIDE sensor chip. In this way, the remote computer can operate the ALPIDE sensor chip and monitor its state.

TCP/IP protocol is a mature and widely used commercial protocol that uses handshake, checksum, acknowledgment, and retransmission mechanisms to improve the reliability of data transmission [15]. SiTCP [16] is a dedicated TCP implementation optimized for physical experiments. It has the advantages of low resource consumption, high transmission rate, and ease of use. The SiTCP allows slow control and data transfer in TCP/IP networks.

The logical block diagram of the SiTCP approach implemented on the main readout board is shown in Fig. 11, where the SiTCP protocol is implemented through the FPGA logic resources and the Ethernet physical layer (PHY) is implemented through the high-speed serial transceiver of the FPGA. The Ethernet PHY reads out the data packets which are pushed into a FIFO. The network packets are routed inside the network and reach the remote computer.

There is an electrically erasable programmable read-only memory (EEPROM) on the main readout board, which can store the Ethernet MAC address, IP address, and port number parameters. The main readout board also has a group of dual inline package (DIP) switches that allows the user to directly modify the lowest three bits of the IP address. Therefore, eight different IP addresses can be selected through the DIP switches under the identical software and firmware configuration.

D. Trigger and Clock Module

The new beam telescope needs to achieve a trigger rate up to 100 kHz. The AIDA2020-TLU can operate with a sustained particle rate of 1 MHz and with instantaneous rates up to 20 MHz [14], which is sufficient for our requirements. The trigger approach shown in Fig. 3 is the same as that

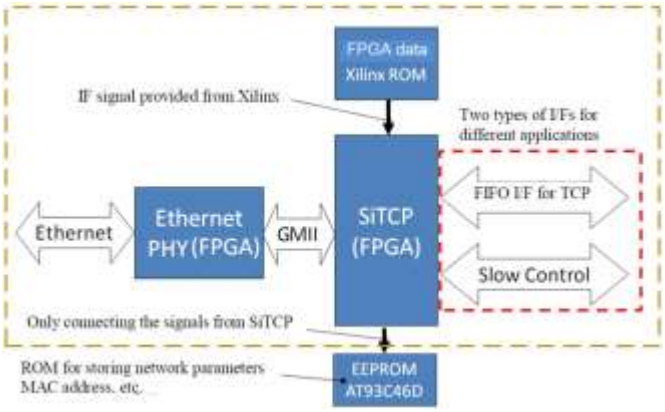

Fig. 11. Logic block diagram of the SiTCP approach.

Fig. 12. Photograph of the fan-out board. A variety of fan-out boards including eight-channel and four-channel boards were designed and the high-definition multimedia interface (HDMI) socket models have been successfully replaced. The figure shows only one of them.

of the EUDET-style beam telescope. The AIDA2020-TLU has several input channels of scintillators and four trigger interfaces. To keep enough trigger interfaces for the DUT, trigger fan-out boards that could fan-out one trigger channel to several channels were made. The remaining three interfaces of the AIDA2020-TLU are available for the DUTs. A photograph of the fan-out board is shown in Fig. 12.

A couple of cross-clock domain problems need to be addressed. The clock approaching diagram is shown in Fig. 13. There are three clock domains, the local clock domain generated by the oscillator, the TLU clock domain, and the ALPIDE clock domain recovered from the data. For slow control signals or single-bit signals, multilevel registers are used to handle cross-clock domains. Asynchronous FIFOs are used for cross-clock domain processing of data stream signals. The TLU trigger signal is connected to the DCTRL control module and the data read module through different multilevel registers. The opcodes (including triggers) and ALPIDE configuration information from DCTRL control module are transferred to the ALPIDE through multilevel registers as well. The configured ALPIDE chip receives the trigger and outputs the serial data stream. This data is recovered out of the clock domain which is used for data processing and packing. The packed data are transferred to the high-speed transceiver via an asynchronous FIFO.

E. Data Acquisition

The data acquisition system is compatible with the readout of the EUDET-style beam telescope. The current EUDAQ2

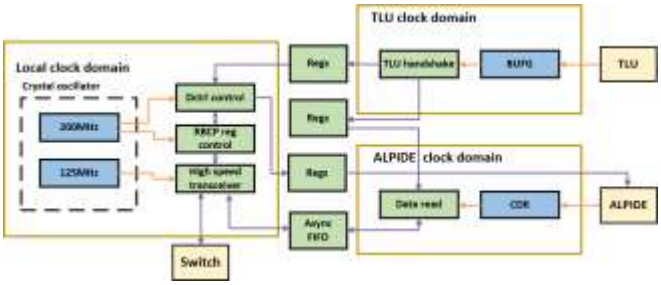

Fig. 13. Clock approaching diagram. There are three clock domains. The TLU trigger signal is connected to the DCTRL control module and the data read module through different multilevel registers. The DCTRL signals are transferred to the ALPIDE through multilevel registers as well. The data are transferred to the high-speed transceiver via an asynchronous FIFO.

data acquisition software is flexible and scalable and widely used for beam telescope systems. To facilitate the migration of experimental beam users, the existing EUDAQ2 software is used to collect data for offline track reconstruction. Due to the low fake hit rate of the ALPIDE sensor chip in the new beam telescope, the tracking environment is cleaner hence the track reconstruction is significantly simplified compared with the EUDET-style telescope.

IV. Performance Tests

A. Plane Electronics Validation

To validate the performance of the single-plane electronics of the telescope system, we employed DESY's existing EUDET-style beam telescope for validation. The photograph of the test setup is shown in Fig. 14. In addition to the beam telescope built from the Mimosa26 chip, there are two ALPIDE planes and one FE-I4 [17] plane. The FE-I4 is designed for the ATLAS experiments with a relatively higher rate capability. The core component of the FE-I4 plane is a hybrid pixel sensor which consists of a pixel sensor with the pixel size of 250×50 μm [17] and a readout ASIC. Since the single-frame readout time window of Mimosa26 is about 112.5μs, much longer than the 5–10 μs of ALPIDE, the particle tracks detected by the EUDET-style telescope plane may not all arrive within the time window of an ALPIDE readout frame. When the detection efficiency of the telescope plane is estimated, the tracks reconstructed by EUTelescope [18] software are required to arrive within the ALPIDE time window. The FE-I4 is employed to implement the function of filtering reconstructed tracks, and its time window is configured to 4μs. It can be assumed that the track event containing the hit from the FE-I4 plane arrives within the ALPIDE time window. As shown in Fig. 14, one ALPIDE plane is installed in the middle as a DUT to verify the single-plane electronics. Another ALPIDE plane was installed at the end to verify the performance of multiple telescope planes working in concert.

Generated by the EUDAQ2 online monitor during data taking, the accumulated 2-D distribution of the fired pixel indices for ALPIDE 1 plane is shown in Fig. 15. The ALPIDE trigger is generated by the coincidence of two pairs of scintillators placed crosswise at the front and back, as shown in Fig. 3. The denser square of hits can be seen as the projection in the plane

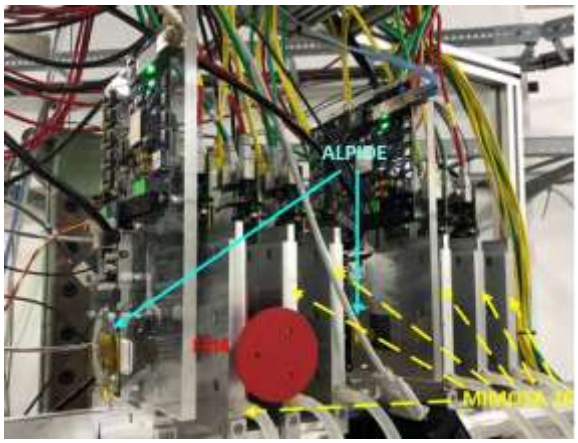

Fig. 14. Single-plane electronics beam test for validation. The Mimosa26 planes are placed with a distance of 50 mm. The telescope planes are spaced 70 mm from the Mimosa26 planes on either side (or unilaterally). The FE-I4 planes are spaced 10 mm from their nearest Mimosa26 planes.

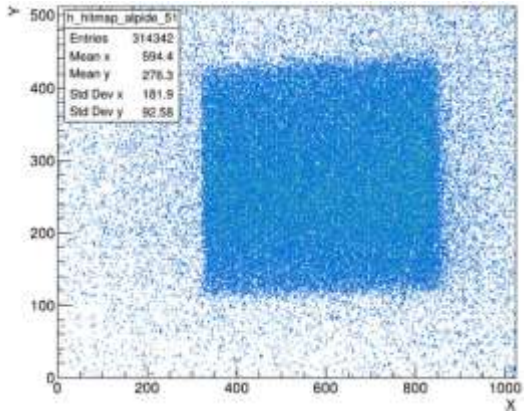

Fig. 15. Two-dimensional distribution of the pixel indices of the data of the hit events for ALPIDE 1 provided by EUDAQ2 online monitor.

of the detector of the overlapping shape of the scintillators along the beam direction. The detector plane is not strictly perpendicular to the beam direction due to manual installation errors. This causes the dense square seems slightly rotated. The hits outside the dense quadrangle are mostly arising from multiple hits in the time window of a single trigger.

B. Full Beam Telescope Test

A full ALPIDE beam telescope consisting of six planes was built after verifying the readout electronics of a single telescope plane. A photograph of the telescope is shown in Fig. 16. In the beam test at the DESY test beam facility with 5 GeV electron, a total of about 1.1 million trigger events were measured.

The correlation between the hit coordinates of the beam particle on different planes allows fast verification of the beam telescope. Fig. 17 shows the clear correlation between the hit coordinate in the *y*-direction on the sixth plane of the beam telescope and that on each of the remaining five planes. The width of the band is correlated with the correlation and density of hit events. The increased density of hit events makes the band brighter and thus visually wider. A worse correlation will also make the band wider. The closer planes have a stronger

Fig. 16. Photograph of six-ALPIDE-plane beam telescope (the DUT is not installed). All planes are equidistantly mounted. The distance between each plane is 46 mm.

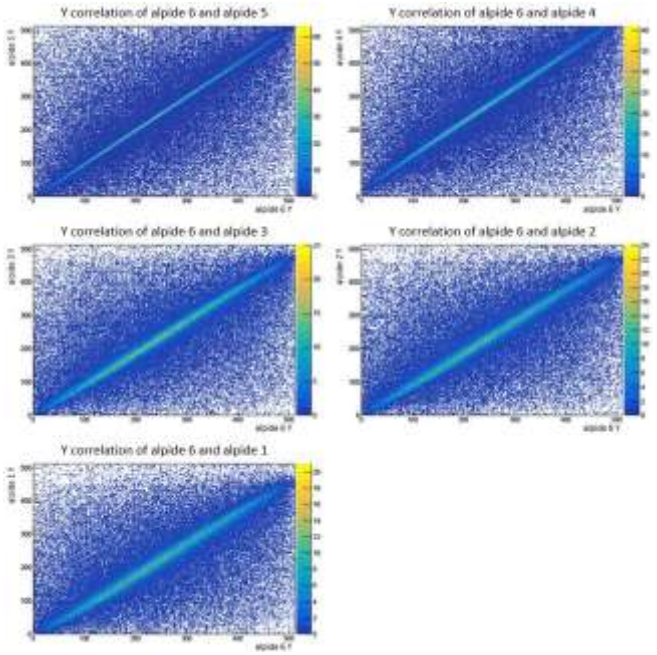

Fig. 17. Correlation between the hit coordinate in the *y*-direction on the sixth plane of the beam telescope and that on each of the remaining planes. The five subfigures are the correlation between ALPIDE 6 and ALPIDE 1 to ALPIDE 5 in the *y*-direction of trigger events, respectively.

correlation due to less scattering of the electrons as they cross the telescope planes. Fig. 15 illustrates that the beam is not directly incident on the center of the sensor plane because of errors during installation. This error can result in some experiments in which the center of symmetry of the band is not in the middle of the image.

Due to the presence of fake hits and multiple hits, the hits belonging to the same trigger event on each plane need to be selected for the track reconstruction. First, the initial selection is done based on the relative spatial positions of the hits of each plane, and then the selected hits are used to perform rough track reconstruction on each of the three planes of the two arms, and the angle between the two tracks called triplet slope is calculated. In the time of matching two triplets, a cutoff value is set for triplet slope to reject any fake triplet. The events exceeding the cutoff value will be discarded.

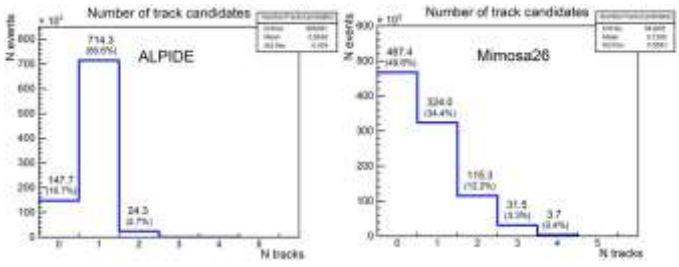

Fig. 18. Histograms of the number of reconstructed tracks per trigger by the ALPIDE beam telescope and the EUDET-style beam telescopes and their frequencies. The probability that the ALPIDE beam telescope can reconstruct 0, 1, and multiple (≥2) tracks in a near-a-million events test is 16.7%, 80.6%, and 2.7%, respectively. This figure is 49.6%, 34.4%, and 16.0% for the EUDET-style beam telescope at the same test beam line setup.

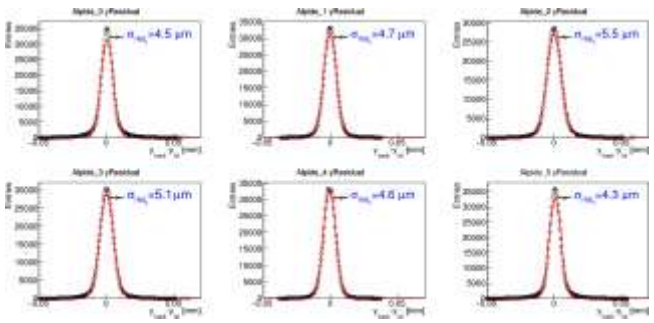

Fig. 19. Distributions of the biased residual in the *y*-direction on the six telescope planes using one million instances with 6 GeV electron beam.

The number of reconstructed tracks per trigger is counted. The comparison between ALPIDE and EUDET-style beam telescopes is shown in Fig. 18. For the EUDET-style telescope, there is a 49.6% probability of having no reconstructed track in a trigger event. But for the ALPIDE beam telescope, the probability is 16.7%. The proportion of trigger events that can be reconstructed with at least one reconstructed track is regarded as the efficiency of the acquired data, which stands for the utilization of the beam. The track reconstruction efficiency of the ALPIDE beam telescope data is 83.3%, which is greater than the 50.4% of the EUDET-style beam telescope. This is due to the low fake hit rate of the ALPIDE chip.

The biased residual is defined as the distance between the fit position of the track on a plane and the measured position of the hit on the plane. The standard deviation of the residual distribution is hereafter denoted as the residual width [8], [19]. The distributions of the biased residual on the telescope planes in a 6 GeV electron beam test are shown in Fig. 19 [8], [18]. Since the size difference between the *x* - and *y*-direction of the pixels is not significant, the distribution of the biased residual in the *x* -direction is similar to that in the *y*-direction. The biased resolutions of distributions in the *x* - and *y*-directions in a 6 GeV electron beam are both measured to be about 5 μm.

When testing the upper limit of the trigger rate, the internal trigger mode of AIDA2020-TLU was used. The trigger rate was gradually increased from 100 kHz and whether the ALPIDE data could be fully obtained by EUDAQ2 software was studied. According to the test, the beam telescope can still work properly under the trigger rate of 220 kHz, i.e., the ALPIDE beam telescope meets the requirements of the design specifications.

TABLE I

COMPARISON BETWEEN ALPIDE TELESCOPE SYSTEM AND EUDET TELESCOPE SYSTEM

Parameter	ALPIDE telescope system	EUDET telescope system
Trigger rate (kHz)	100	3.9
Sensitive area (mm^2)	414	224
Residual distribution(μm @ 6 GeV)	~5	~3

Summarizing the parametric performance of the ALPIDE beam telescope and the EUDET-style beam telescope as shown in Table I, the ALPIDE beam telescope has a 50 times higher trigger rate as well as a much lower fake hit rate compared to the EUDET-style beam telescope. The sensitive area of the new telescope is also larger. The biased residual of ALPIDE beam telescope is about 1.5 times larger than that of the EUDET-style beam telescope, which is compatible with the difference of pixel pitch between Mimosa26 and ALPIDE.

Stability tests were also carried out. The ALPIDE beam telescope was installed on the beam line for a week. Several validation experiments were carried out during this period. The electronics did not show any abnormalities.

V. CONCLUSION

By studying and selecting MAPS chips, establishing the telescope simulation model, designing the verification circuit, and testing the electronics, a new beam telescope was set up. It has a 100 kHz trigger rate, a low fake hit rate, 414 mm^2 sensitive area, and about 5μm biased resolution. In addition, the new telescope facilitates not only more efficient utilization of the test beam but also a cleaner environment for track reconstruction compared to the EUDET-style beam telescope. This beam telescope meets the requirements of the next generation of beam telescope with DESY II and it has been installed at the DESY test beam facility's T22 beam line for further optimization of the system performance.

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