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Design and Performance of the mDOM Mainboard for the IceCube Upgrade

The IceCube Collaboration

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About 400 mDOMs (multi-PMT Digital Optical Modules) will be deployed as part of the IceCube Upgrade project. The mDOM's high pressure-resistant glass sphere houses 24 photomultiplier tubes (PMTs), 3 cameras, 10 flasher LEDs and various sensors. The mDOM mainboard design was challenging due to the limited available volume and demanding engineering requirements, like the maximum overall power consumption, a minimum trigger threshold of 0.2 photoelectrons (PE), the dynamic range and the linearity requirements. Another challenge was the FPGA firmware design, handling of about 35 Gbit/s of continuous ADC data from the digitization of the 24 PMT channels, the control of a high speed dynamic buffer and the discriminator output sampling rate of about 1 GSPS. High-speed sampling of each of the discriminator outputs at ~1 GSPS improves the leading-edge time resolution for the PMT waveforms. An MCU (microcontroller unit) coordinates the data taking, the data exchange with the surface and the sensor readout. Both the FPGA firmware and MCU software can be updated remotely. After discussing the main hardware blocks and the analog frontend (AFE) design, test results will be shown, covering especially the AFE performance. Additionally, the functionality of various sensors and modules will be evaluated.

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1. Introduction

The IceCube Upgrade detector [1] will be installed in the 2025/26 austral summer at the geographic South Pole in the center of the existing IceCube Neutrino Observatory. The IceCube Upgrade will enable precision measurements of neutrino properties, allow improved calibration of the IceCube array, and serve as a technology test platform for the future IceCube-Gen2 project. IceCube Upgrade will comprise about 700 optical sensors on seven strings. Among these sensors, 402 are mDOMs (multi-PMT Digital Optical Modules) [2]. Each mDOM features 24 3-inch photomultiplier tubes (PMTs), read out individually with a 120 MSPS 12-bit ADC. Single-channel triggers are realized with a per-channel discriminator, and nanosecond timing precision is achieved by sampling the discriminator output at 960 MSPS.

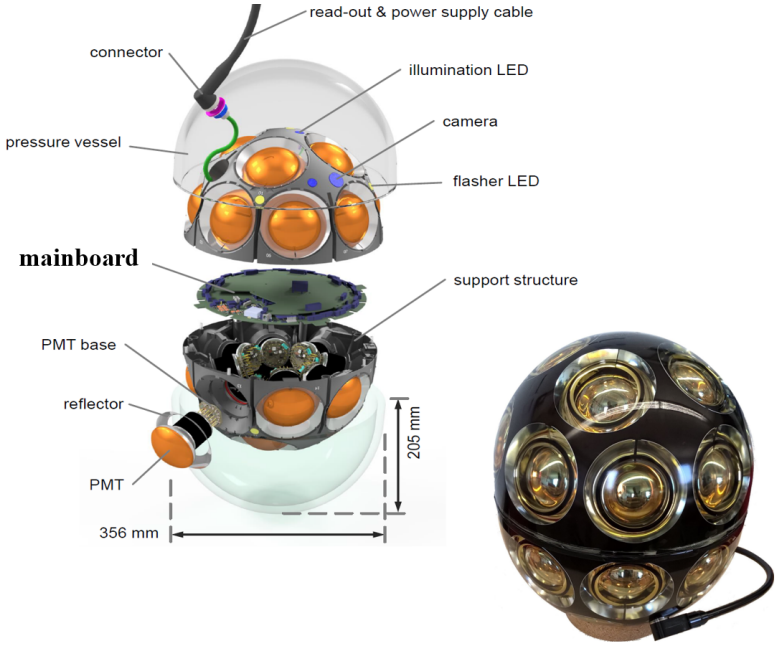

Figure 1: The IceCube Upgrade mDOM, exploded view (left) and photograph (right).

The mDOM mainboard is located in the "equatorial" region of the mDOM. See the exploded mDOM view in Fig. 1. The main components of the mDOM mainboard (Fig. 2) are two DC/DC converters, circuitry to monitor currents and voltages, 24 analog front-end (AFE) channels, a 2 Gbit DDR3-RAM-based event buffer, a powerful FPGA, an MCU (Microcontroller Unit), the ICM (IceCube Communication Module), a Xilinx CPLD, various sensors (Fig. 3) and the mDAB (mDOM Adapter Board, Fig. 8). When taking data at a sampling rate of 120 MSPS, the power consumption of the mDOM is about 9 W.

2. The Power Supplies

A single wire pair is being used to carry the DC power and communication signals of the mDOM. The isolating primary DC/DC converter, featuring a wide input range from 36 V to 160 V,

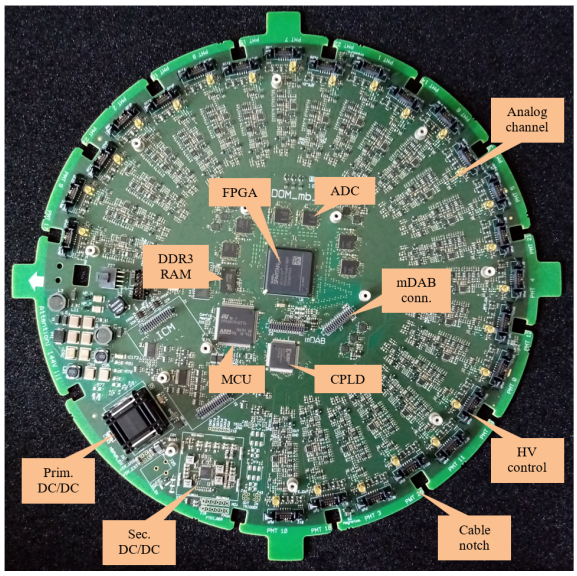

Figure 2: Photograph of an assembled mDOM mainboard, with major components labeled.

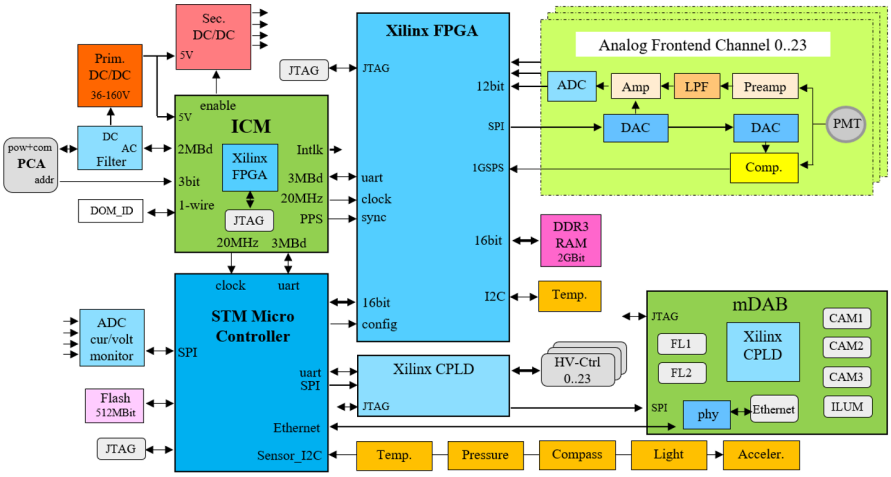

Figure 3: mDOM mainboard block diagram.

generates 5 V. The secondary DC/DC converter, an ADP5014ACPZ, converts the 5 V into four voltages of the range from 1 V to 3.3 V. It also controls the power on/off sequence of the four power rails (Fig. 4), like it is recommended for Xilinx Spartan 7 FPGAs.

Besides the proper on/off sequence, a very low noise level on the power rails is important as well, especially for the 1.8 V and the 3.3 V, partly being used to supply the analog frontend circuitry. An AC-coupled differential probe has been used to measure the noise levels (Fig. 5). For comparison the probe was shorted to GND first. The noise levels seen are very low, less than 2 mV pk-pk in a frequency range from DC to 1 GHz.

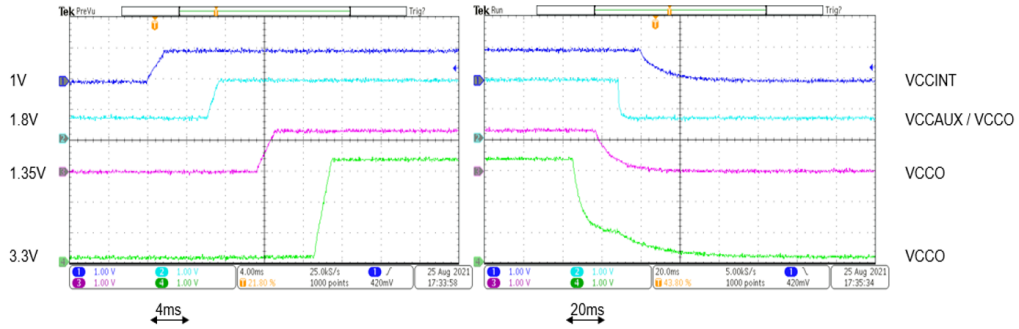

Figure 4: Secondary DC/DC converter, measured the power on/off sequence using a scope.

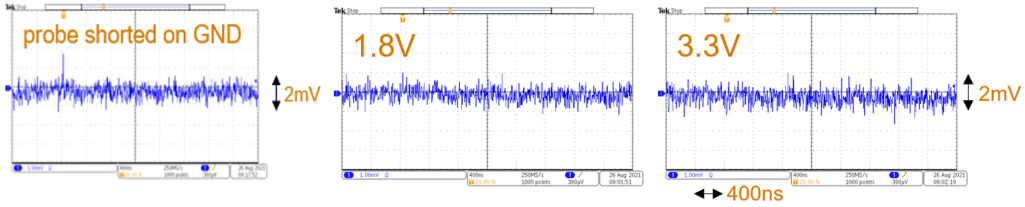

Figure 5: Secondary DC/DC converter, scope noise measurements on two analog voltage rails.

3. The ICM

The ICM (IceCube Communication Module, Fig. 6 left) is a universal piggy back module, being used by all IceCube Upgrade in-ice devices. A filter on the mainboard recovers the communication signal, modulated on the mDOM DC power. The primary component of the ICM is a Xilinx Spartan 7 FPGA. After power-on, the FPGA loads a write-protected "golden image". Initiated by a software command, the FPGA loads a runtime image from another flash page afterwards. The runtime images can be remotely updated at any time. In case of a corrupted golden image, the FPGA tries to load a second, also write protected copy of the golden image. The ICM block diagram is shown in Fig. 6.

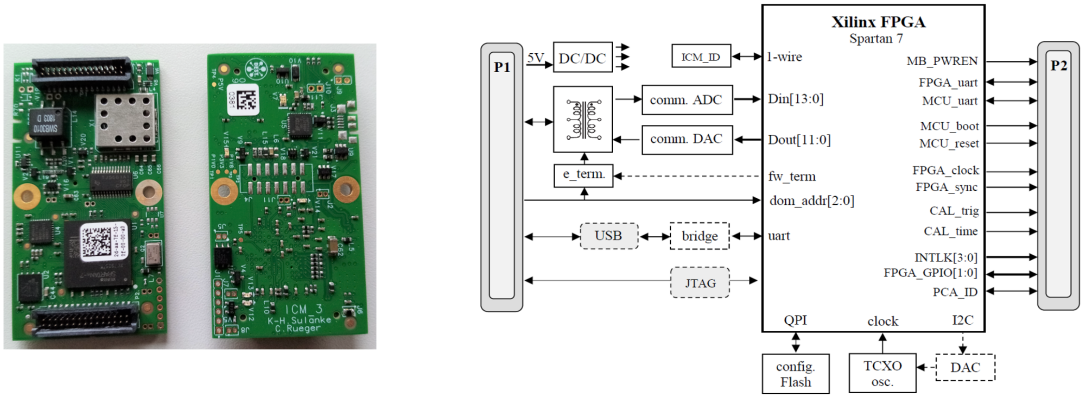

Figure 6: Photo and block diagram of the IceCube Communications Module (ICM).

After powering on a wire pair, only the ICM is powered on by default. Once the communication to the surface has been established, the next step is to enable the secondary DC/DC converter by an ICM command. Four interlock signals, like e.g. "High Voltage Enable", are directly controlled by the ICM. A precision, low phase noise, temperature-compensated oscillator provides the 20 MHz system clock to the MCU and the FPGA. The low phase noise of the oscillator is important to guarantee the accurate time calibration, required for nanosecond-precision event timestamping. Data exchange, mainly between the ICM and the MCU, takes place through a UART channel running at 3 MBd.

The half-duplex communication signal is ASK-encoded. A trapezoidal-shaped bipolar pulse encodes a binary "1", while a quiet line encodes a "0". Figure 7 shows the 2 MBd communication signals, measured at both ends of a 2800 m-length IceCube cable.

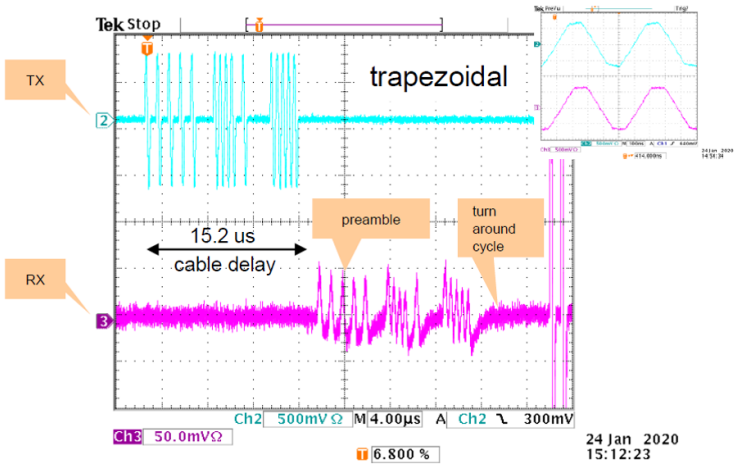

Figure 7: Wire pair communications signals at transmission (top) and reception (bottom) over a 2800 m-long cable.

4. The MCU

The microcontroller (MCU) is an STM32 of the type STM32H743ZIT6. Key features are a 32-bit Arm® Cortex®-M7 core with double-precision FPU, L1 cache (16 Kbytes of data and 16 Kbytes of instruction), a clock frequency up to 400 MHz, internal 2 Mbyte flash memory and 1 Mbyte RAM.

Once powered, the MCU boots from its flash, loading the mainboard FPGA afterwards. The FPGA is mapped into the MCU's address range, like an external memory device, to be accessed via a 16-bit data bus. Before collecting event data, the MCU initializes the AFE channels and sets the high voltage of the PMTs. The PMT-base UART connection, multiplexed by a Xilinx CPLD to the MCUs UART, allows setting and monitoring the PMT's high voltage. An SPI bus is used to individually enable power to any of the AFE channels. The same bus also controls the mDAB board. A second SPI bus is used to gather power supply monitoring data. Temperature, pressure, compass, light and accelerometer sensors are controlled by an I^2C bus. A 3 MBd UART connection is used for the data traffic to the ICM.

5. The mDAB

The mDOM Adapter Board (Fig. 8) is primarily needed to accommodate the connectors of three attached cameras, an illumination board and two LED flasher daisy chains. A Xilinx CPLD is translating the SPI bus commands of the MCU into power-enables and flasher-select signals. The ethernet connection is an option for test setups in the lab. Besides camera readout by SPI bus and flasher control, the mDAB also serves as a heat sink for the FPGA, lowering the FPGA-chip temperature by 10K. In addition the mDAB acts as a shield due to its GND-layer, protection the surrounding PMTs against EMI caused by the power supplies and the digital circuitry.

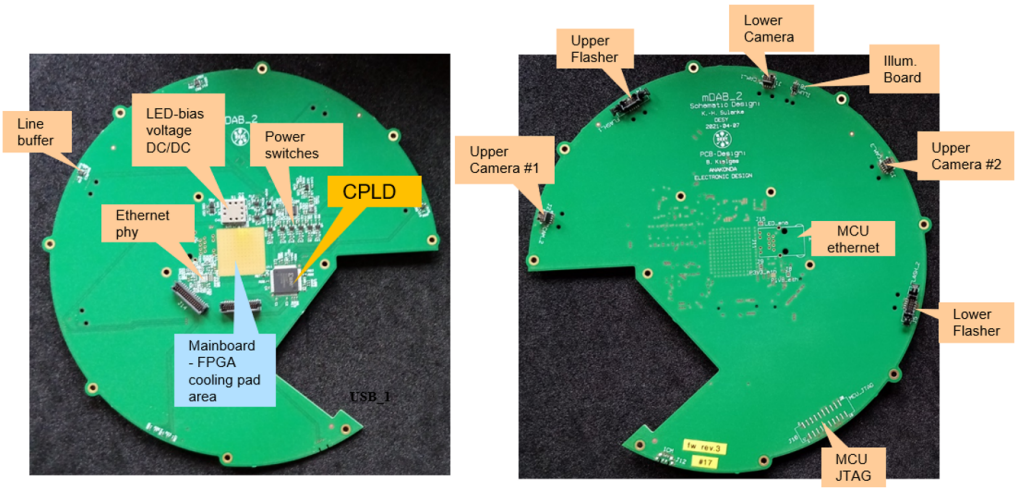

Figure 8: Photographs of the mDOM adapter board: bottom view (left) ans top view (right).

6. The FPGA

The FPGA, a 676-pin BGA chip, is a Xilinx Spartan 7 XC7S100-2FGGA676I. Its main task is the readout of 24 analog front-end channels. The ADC baselines and trigger thresholds are set by the MCU through the FPGA. The serial ADC data, 48 serial bitstreams at 720 Mbit/s, result in an overall data rate of 34.56 Gbit/s. These bitstreams are continuously decoded and buffered. In case of a trigger, the corresponding data are propagated to the event buffer. The DDR3-RAM-based buffer, connected to the FPGA and organized as a ring buffer, allows the mDOM to store a sufficient amount of data to deal with any intermittent readout delays by the surface data acquisition software. The 24 ToT (time over threshold) signals, provided by the discriminators, are sampled at 960 MSPS, resulting in a leading-edge time resolution of about 1 ns.

7. The Analog Frontend

Most challenging for the analog frontend design was to accomplish a very low power consumption while maintaining enough bandwidth, sufficient dynamic range and a good linearity. Low noise in the neighborhood of EMI-causing digital parts like DC/DC converters, the MCU, the FPGA and

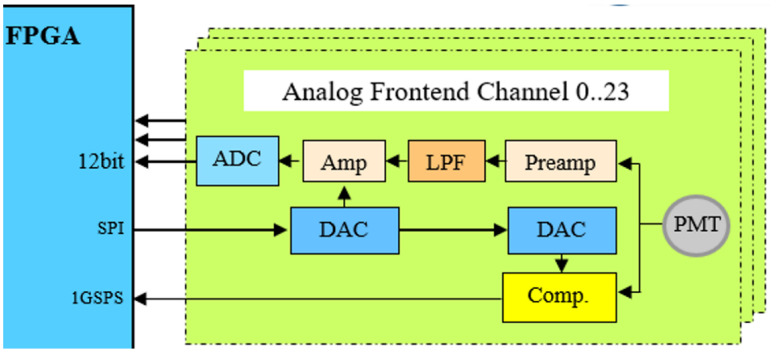

Figure 9: Block diagram of the Analog Frontend (AFE) circuit.

the DDR3 RAM was achieved by a careful design of the power supply and the PCB. The ADC baseline noise for all 24 channels is typically below 0.7 lsb RMS.

In contrast to traditional PMT readout designs with an AC-coupled input, we deal here with a fully DC-coupled approach. This avoids any signal droop effects (ADC-baseline variations) depending on the time between consecutive PMT pulses. Figure 9 shows the block diagram of the AFE. The PMT signal is directly connected to the discriminator (Comp.) and the preamplifier. Two precise 16-bit DAC channels are used to adjust the discriminator threshold and the ADC baseline. For pulse shaping a low pass filters is being used. Precision (0.1%) gain setting resistors are chosen. The dynamic range reaches from 0.2 PE to 150 PE. Figure 10 shows the comparison of simulation and measurement for a SPE-like pulse at an ADC sampling rate of 120 MSPS.

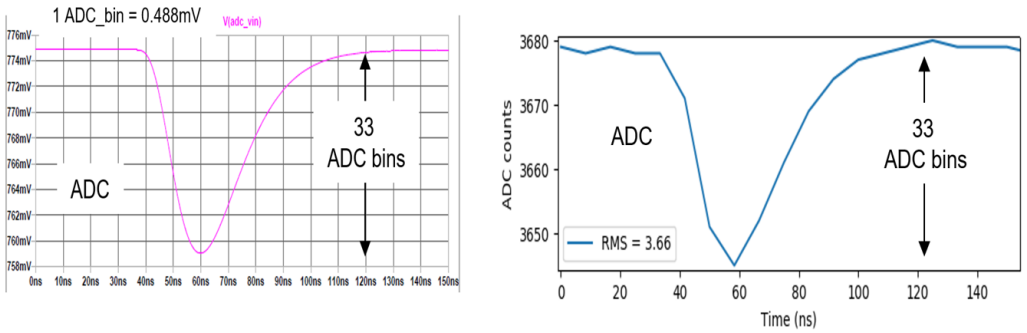

Figure 10: SPE like pulse, and simulated (left) and measured (right).

Figure 11 shows ADC readout and double pulse resolution of the discriminator for 0.2PE and 1PE signals. The double-pulse resolution of 10 nanoseconds is achievable by using the high-speed discriminator digitization even when the pulses are not separable in the filtered PMT signal.

Linearity measurements for the analog channel, using a calibrated laser source are depicted in Fig. 12. The required range was 100 PE. The saturation is caused by the AFE amplifiers.

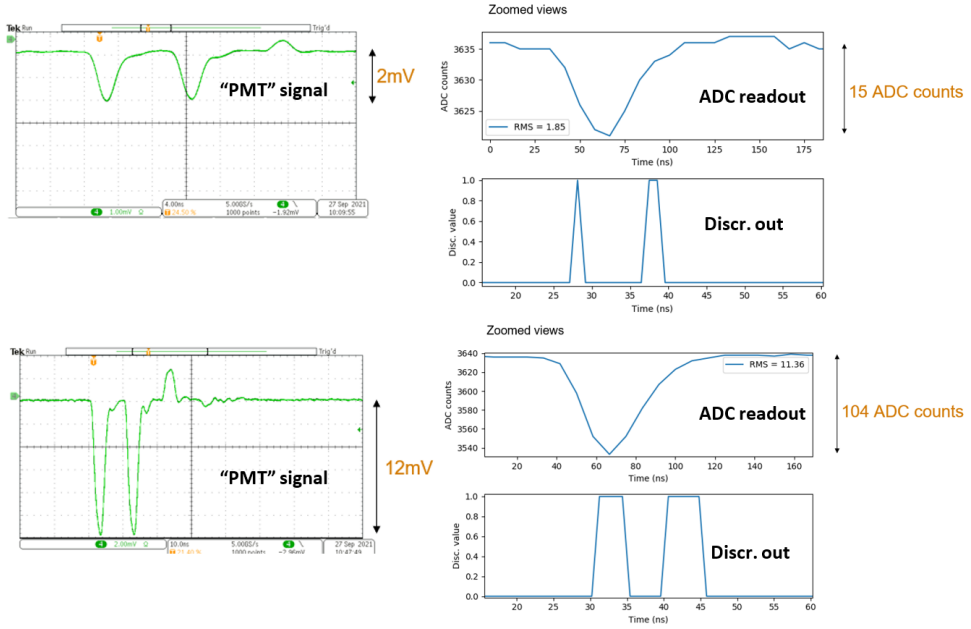

Figure 11: The PMT-pulse discriminator, 10 ns-double-pulse-resolution for 0.2 PE (top) and 1 PE (bottom).

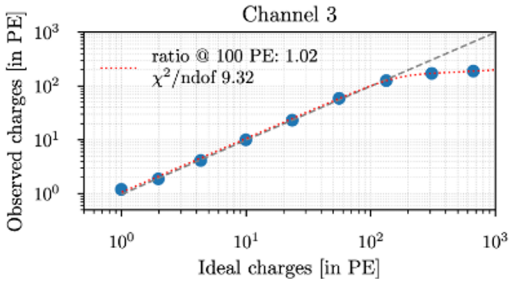

Figure 12: The AFE linearity measurement, using a calibrated laser source.

8. Conclusions and Status

The design fulfills the engineering requirements, e.g. operational temperature range, maximum AFE noise level, AFE linearity, data buffer size and event time resolution [3]. About 40 mDOM mainboards have been extensively tested so far. Each mainboard underwent a thermal shocks between −40°C and +70°C. No failures have been observed after the stress tests. Presently the first batch of mainboards is being integrated into mDOMs, to be tested again during the final acceptance test (FAT) [3].

References

[1] **IceCube** Collaboration *PoS* **ICRC2019** (2019) 1031.

[2] **IceCube** Collaboration *PoS* **ICRC2021** (2021) 1070.

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