Development of the Continuous Readout Digitising Imager Array Detector

A. Marras,[a,b,1] **A. Klujev,**[a,b] **S. Lange,**[a,b] **T. Laurus,**[a,b] **D. Pennicard,**[a,b] **U. Trunk,**[a,b] **C. B. Wunderer,**[a,b] **H. Krueger,**[c] **and H. Graafsma**[a,b,d]

[a] *Deutsches Elektronen-Synchrotron DESY, Germany*
[b] *Center for Free-Electron Laser Science CFEL, Germany*
[c] *University of Bonn, Bonn, Germany*
[d] *Mid Sweden University, Sundsvall, Sweden*
E-mail: alessandro.marras@desy.de

ABSTRACT: The CoRDIA project aims to develop an X-ray imager capable of continuous operation in excess of 100 kframe/s. The goal is to provide a suitable instrument for Photon Science experiments at diffraction-limited Synchrotron Rings and Free Electron Lasers considering Continuous Wave operation. Several chip prototypes were designed in a 65nm process: characterization has so far confirmed expected performances of basic circuital blocks.

KEYWORDS: Detector; X-ray; Photon Science.

[1] Corresponding author.

Contents

1 Introduction

Detectors available today for Photon Science X-ray experiments are roughly divided between the ones optimized for Synchrotron Rings (SRs) and low-repetition-rate Free Electron Lasers (LR-FELs) and the ones optimized for high-repetition-rate FELs (HR-FELs). Detectors in the first category are typically capable of continuous acquisition up to a few k-frame/s (typical examples: [1], [2]). A common approach for detectors in the second category ([3],[4],[5]) is to acquire a "burst" of images and store them in an internal memory on the readout ASIC: the data are then read out slowly during the gap between adjacent FEL trains, while the image acquisition is paused. Thus they can achieve substatially higher rate (up to the MHz regime), but only for short (a few hundred images) bursts.

The upgrade of SRs toward the diffraction limit is expected to increase brilliance by 2 orders of magnitude and demands an upgrade of X-ray imagers to be proportionally faster, while maintaining their continuous acquisition capability. Such devices are also needed to exploit the potential of HR-FELs considering Continuous Wave operation, that will no longer provide gaps between trains which are long enough to read-out an internally-stored image-burst.

2 CoRDIA

The CoRDIA (Continuous Readout Digitising Imager Array) detector aims at providing a hybrid detector capable of photon discrimination at 12 keV (also compatible with high-Z sensors for higher energies), a substantial full well, a compact pixel size (~110um), and continuous readout capability at a frame rate of ~150 kfr/s.

2.1 Readout ASIC Architecture

The imager is a hybrid pixel detector, where a sensor (n-on-p Silicon or High-Z material) is bump-bonded to a readout ASIC. The readout ASIC consists in a 2D pixel array containing a circuital chain of analog (charge integrating) Front Ends (FEs), Analog-to-Digital converters (ADC), and readout (RO) stages.

The circuit stages are pipelined so to obtain a Continuous Writing-Reading (CWR) sequence, where the chip readout does not impose pauses in the image acquisition. This has also the advantage of eliminating the need for a large embedded in-pixel memory, thus reducing the pixel size with respect to burst-mode imagers optimized for HR-FELs. Since the data readout needs to happen at a frequency compatible with the acquisition frame rate, high-speed drivers were included in the design, along with suitable circuits preparing the image data for high-speed readout.

Digital-to-analog conversion happens on a battery of ADCs distributed in the pixel array, as analog signals would not be suitable for high-speed readout. Both the data digitization and its readout require a non-negligible time, which would risk restricting the fraction of time during which the detector can react to new photons: the CWR approach overcomes this limitation by using a pipelined architecture (Figure 1) of the charge-integrating and signal-processing circuits, so that while one image is being integrated by the FE, the former image is digitized by the ADC and streamed out. This approach reintroduces the need for a small memory inside the detector, to allow the two operations to happen in parallel; but since such memory depth is very small (just two images), it does not inflate the pixel size significantly.

The Analog FE receiving charge photogenerated in the sensor consists of an Adaptive Gain charge-integrating amplifier capable of extending its dynamic range by modulating its response on the basis of the incoming flux, in real time (as, for example, in [3]). The circuit integrates the charge alternating between two sets of capacitors so that, while one set is used to acquire an image, the other set, containing the integrated charge relative to the former image is used as an input for a Correlated-Double Sampling (CDS) circuit, and then an ADC. As soon as bits are produced by the ADC, they are encoded and streamed out through the RO stage.

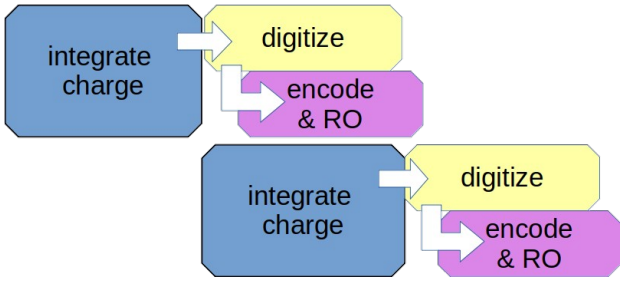

Figure 1. CoRDIA pipelined architecture

2.2 Prototypes

Several chip prototypes (Figure 2) were designed in TSMC65nm technology, and manufactured by means of Multi-Project Wafer (MPW) runs, to test and validate circuit blocks and circuital chains.

In 2021 a first (CoRDIA_01) prototype was designed and manufactured to validate the analog FEs. It consists in separate test structures for the Adaptive Gain circuit, CDS block, the circuit to alternate between two readout sub-chains (to achieve CWR), and a full circuital chain of these blocks. The analog blocks described were designed in a Standard-Cell fashion for ease of re-usability and rearrangement, and sized to be easily interfaced to a digital Standard Cell array in the same technology. Provisions were made to improve the design yield, as well as to improve circuit resilience to Total Dose Ionizing damage, along RD53 recommendations for the

technology. Tests in 2022 confirmed the expected performance for the Adaptive Gain circuit at the expected frame rate of 150kfr/s (as shown in [6]).

In parallel, a second (HSI_ADC01) prototype has been designed and manufactured. It included several ADC variants based on a 11-bit Successive Approximation Register (SAR) architecture. In the CoRDIA design, one ADC is expected to serve serially 16 pixels, thus the ADC need to be capable of at least 16×150k= 2.4MS/s. Tests in 2022 [6] confirmed the expected performance at 2.5MS/s, while retaining a 10b Effective Number Of Bits (ENOB) resolution.

During 2022 a third (CoRDIA_02) prototype has also been designed, embedding multiple FEs and an ADC into a modular “superpixel” structure that can be repeated to form the pixel array. About half of the 400 um×400 um "superpixel" layout is used for 16 FE circuits, one quarter is used for the ADC, and another quarter is reserved for a fraction of the common RO stage that is meant to encode and read-out the output of 128 ADCs (2k pixels). The superpixels are arranged in a mirrored double-column fashion around the common silicon area reserved for the RO circuit. The bump-bond pads interfacing to the sensor are redistributed to a uniform 2D array to facilitate bonding: thus each 400 um×400 um "superpixel" is interfaced as a 4×4 array of pixels with a 100um pitch. We plan to relax this pitch to 110um in future designs, to be compatible with available sensors. Each FE circuit is also equipped with an internal calibration circuit that can be used to emulate the detection of a given number of photons, for fast characterization of the detector. The goal of the prototype is to verify the signal-processing of images in a pipeline fashion. The prototype has been manufactured at the beginning of 2023 and is currently under test; preliminary results confirm basic circuit functionality.

During 2023 a further (CoRDIA_03) prototype has been designed, including two different variants of the RO circuit. The RO architecture has been developed by NIKHEF for the Timepix4 chip, and consists in a Physical Coding Sublayer (PCS) circuit to encode the signal (64b/66b) and a Gigabit Wire Transmitter (GWT) as a fast driver. The circuit topology has been extensively tested by the Timepix collaboration both at 5.12 Gb/s and at 10.24 Gb/s [7]. Even at the lower bit rate (5.12 Gb/s) it would be suitable for the CoRDIA needs, as it is capable of streaming out the output of 128 ADC (2k pixels) at the required frame rate. In this prototype, we have adapted the RO circuit to the fan-in expected within the CoRDIA structure, and we have adapted it to our layout constraints (so that the the RO circuit fits in the space allocated for it in the "superpixel" structure). The prototype is being manufactured, and it is foreseen to be tested in 2024.

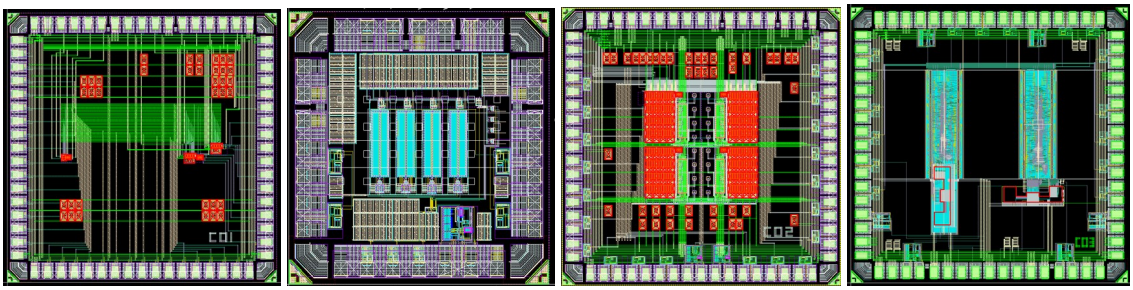

Figure 2. Layout of the CoRDIA prototypes. Left-to-right: CoRDIA_01, HSI_ADC01, CoRDIA_02, CoRDIA_03

3 Conclusions and future steps

Several prototypes were designed to test circuital blocks and block chains for the CoRDIA detector. Tests are in progress, but have so far confirmed expectations.

Once the tests on these prototypes confirm desired performance, a pixel array of reduced dimensions will be designed, integrating all the previously tested circuits in a matrix of complete "superpixels". This is expected to happen in 2024.

Our objective is to have a full-sized detector ready by the start of operation of the upgraded Petra IV SR, expected in 2029.

Acknowledgments

The authors would like to acknowledge:

the Caribou team at DESY (in particular S. Spannagel and T. Vanat), for providing a versatile system for prototype testing;

NIKHEF (particularly V. Gromov and A. Vitkovskiy), for allowing the authors to include a version of the PCS-GWT circuit in the CoRDIA design, for fast data streamout;

CERN, for allowing the reuse of CMOS IO pads and SOFIC ESD structures in the MPW design;

Europractice, IMEC and CERN for their MPW and design tool support.

References

1 A. Mozzanica et al., *Characterization results of the JUNGFRAU full scale readout ASIC*, J. Instrum. 11 (2) (2016) C02047, 8.

2 D. Pennicard et al., *The LAMBDA photon-counting pixel detector*, J. Phys.: Conf. Ser. 425 (2013) 062010.

3 A. Allahgholi et al., *AGIPD, a high dynamic range fast detector for the European XFEL*, J. Inst. 10 (2015) C01023.

4 M.C. Veale et al., *Characterisation of the High Dynamic Range Large Pixel Detector (LPD) and its use at X-ray Free Electron Laser Sources*, 2017 JINST 12 P12003

5 M. Donato et al., *First functionality tests of a 64 × 64 pixel DSSC sensor module connected to the complete ladder readout*, 2017 *JINST* 12 C03025

6 A. Marras et al., *Development of CoRDIA: An Imaging Detector for next-generation Photon Science X-ray Sources*, Nuclear Inst. and Methods in Physics Research, A 1047 (2023) 167814

7 X. Llopart, et al., *Timepix4, a large area pixel detector readout chip which can be tiled on 4 sides providing sub-200 ps timestamp binning*, JINST 17 (2022) C01044.