MTCA.4-BASED CLOCK AND TIMING DISTRIBUTION FOR PETRA IV

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Abstract

At DESY, the technical design phase to upgrade the PETRA III storage ring towards the 4th-generation synchrotron light source PETRA IV [1] is in full progress. This foresees a complete renewal of the machine including its existing timing and synchronisation system. The new timing and synchronisation system needs to deliver precise clocking, which will be implemented by an application-specific hardware design. Further on, it has to provide trigger signals and beam-synchronous information to the subsystems located across the facility. The main hardware for the timing system will be based on the MTCA.4 standard. This platform has been successfully implemented at DESY / EuXFEL. Because of new specific requirements for PETRA IV, the successor hardware has to be adapted and upgraded to a new design. This paper describes the system design and the facility-wide distribution of precise clocks, trigger signals and timing system-related meta-information.

OVERVIEW OF THE PETRA IV PROJECT

The PETRA storage ring was built in 1978 as an electron-positron collider for high-energy physics experiments and later used as a pre-accelerator for the HERA electron-proton collider. Since 2009, the PETRA accelerator has been part of the third-generation synchrotron radiation facility, PETRA III. In 2016 a research and development program started to pursue the possibility of upgrading the PETRA III accelerator to a state-of-the-art fourth-generation storage ring, PETRA IV, based on stronger focusing lattices utilizing hybrid Multi-Bend Achromats. The upgrade would enable PETRA to produce ultra-low emittance electron beams and provide high brilliance photon beams to photon science experiments. The generated beams would be close to the diffraction limit for X-rays of up to 10 keV, making PETRA IV the ultimate X-ray microscope [1].

The PETRA storage ring has a circumference of 2304 m with eight arcs and four long straight sections. A pre-accelerator chain, consisting of an S-band linear accelerator (LINAC II) with a triode RF gun, a 28.8 m accumulator ring (PIA) for compressing the bunches, and a booster ring (DESY II), injects 6 GeV electron bunches into the PETRA storage ring. Since the emittance of the DESY II booster is much larger than the low-emittance requirement of PETRA IV, the booster ring will be renewed entirely (DESY IV). The other sections of the pre-accelerator chain will be partially refurbished and upgraded.

The photon science capabilities of the new PETRA IV facility will be significantly enhanced by building an entirely new experimental hall hosting additional beamlines in the West area of the PETRA ring in addition to the existing halls in the North, North-East and East areas (see Fig. 1).

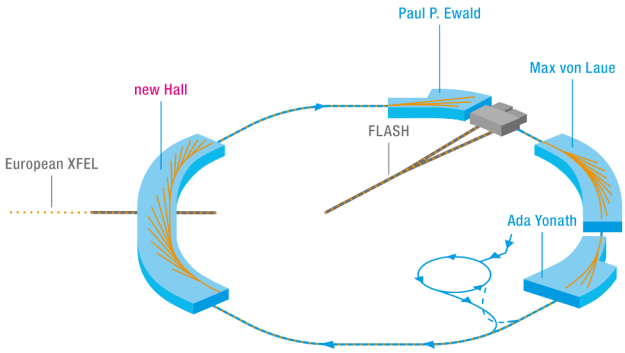

Figure 1: Overview of the future PETRA IV facility.

The renewal of the PETRA infrastructure and machine is accompanied by modernizing the hardware and software of the accelerator controls utilizing state-of-the-art industrial standards and technologies. Many components operated at PETRA III have already been used in previous generations of the storage ring, and their service life has practically elapsed. The implementation of the new PETRA IV system will be based on the MTCA.4 (Micro Telecommunications Computing Architecture) electronics standard [2], the upcoming de facto standard within the accelerator community.

THE PETRA IV TIMING AND RF SYNCHRONISATION SYSTEMS

The timing and RF synchronisation systems are essential functional components of the PETRA IV project, providing synchronisation for operations and processes across the main storage ring, pre-accelerator chain and experimental beamlines.

The RF synchronisation system will provide continuous reference RF signals generated by a unique, stable master oscillator to drive local, low-noise oscillators. The RF fundamental systems of the PETRA IV storage ring and the DESY IV booster require a 500 MHz frequency, while the PETRA IV 3rd harmonic and PIA 4th sub-harmonic RF systems operate at 1.5 GHz and 125 MHz, respectively, both of which will be derived from the 500 MHz RF reference frequency.

The timing system will provide precise accelerator-related timing information and beam-synchronous signals and data to various measurement systems and all beamline experiments across the accelerator facility. The system will use the 500 MHz RF reference to generate and distribute multiple low-jitter machine clocks and event-based trigger signals

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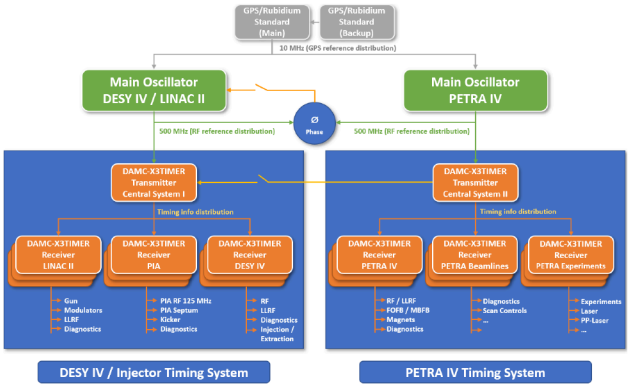

Figure 2: Architecture of the timing and RF synchronisation systems.

(e.g. revolution and bunch triggers, beam injection and extraction signals). In addition, it will distribute information related to machine and beam operation, which is either generated internally (e.g. unique beam revolution number and timestamp for tagging event data) or received from external systems (e.g. machine and beam status; bunch filling pattern; postmortem, injection veto and beam dump signals).

Two central timing and RF synchronisation systems are foreseen, one for the PETRA IV accelerator and the other for the pre-accelerator chain (see Fig. 2). This approach is needed to cope with certain operational modes that require decoupling the activity of the storage ring from the pre-accelerator chain. One such example is the dispersion measurement procedure during which the RF base frequency of PETRA IV will be swept while the pre-acceleration chain will still use the unaltered RF base frequency to prepare the next injection. After the dispersion studies are completed and the RF base frequency of PETRA IV is restored, the two systems will re-synchronise to allow the booster to inject new electrons correctly into the buckets of the storage ring.

THE TIMING SYSTEM ARCHITECTURE

The timing system comprises two central components, located in the Northern supply hall next to the central RF synchronisation system, and multiple local timing systems distributed in a star-like topology that covers all locations along the PETRA IV storage ring, pre-accelerator chain, and experimental halls where timing signals and data must be provided (see Fig. 3).

The central sources will distribute the timing information to the local systems via a redundant, path-compensated optical fibre network. The optical fibres will primarily be routed through the PETRA tunnel sections on dedicated cable trays for easy deployment and potential later enhancement or replacement of individual fibre bundles. For the best performance of the active drift compensation, single-mode optical fibres, suitable for wavelengths ranging from 1270 nm to 1550 nm, and bi-directional optical Small Form-factor Pluggable (SFP) transceivers with wavelength multiplexed transmission and reception on the same fibre will be used.

Each central timing system will comprise a 9U 12-slot MTCA.4 crate equipped with two redundant power supplies, two cooling units, one host CPU AMC (Advanced Mezzanine Card), one MCH (Management Controller Hub) and ten DAMC-X3TIMER modules, the main component of the timing system. In addition, Rear Transition Modules (RTMs) will be developed and mounted on the back of the DAMC-X3TIMER slots to distribute clock and trigger signals to various PETRA IV systems. A second 9U MTCA.4 crate, configured identically and placed in a neighbouring rack, will serve as a backup system. The DAMC-X3TIMER can be configured to operate either as a transmitter, repeater, or receiver. One DAMC-X3TIMER in the first central crate will serve as the heart of the overall timing system, while all the other nine modules will function as repeaters redistributing the timing information to the local systems.

Each local supply hall along the PETRA IV storage ring and pre-accelerator chain will host a temperature-controlled rack holding an MTCA.4 crate, identical to those used by the central systems, for redistributing the timing information. Local clients of the various accelerator subsystems and beamline experiments will be connected to the redistribution crates by optical patch cables. Accelerator subsystems will place their electronics in the same supply halls. In general, those will mostly be MTCA.4 based systems. Hence, a DAMC-X3TIMER plugged into those systems will function as the end receiver and local timing system client. The fibre cable topology will allow receivers with high requirements for the input signals to be connected directly to the transmitter; all others can use the redistribution crates.

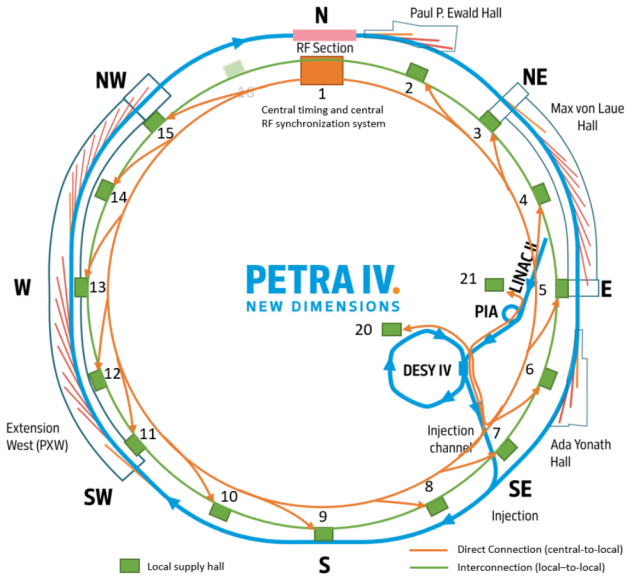

Figure 3: Distribution of the central and local timing systems along the PETRA IV storage ring and pre-accelerator chain.

THE DAMC3-X3TIMER MODULE

The design of the DAMC-X3TIMER module is based on the concept and functionality of the X2TIMER AMC that was developed for and successfully operated at the European XFEL and FLASH facilities [3]. The DAMC-X3TIMER AMC can be configured to operate either as a transmitter, using an external RF reference or an internal oscillator for standalone mode, as a repeater for further distribution or as a receiver for local timing system clients. Figure 4 shows a functional block diagram of the DAMC-X3TIMER.

When configured as a transmitter, the DAMC-X3TIMER will assemble a timing event data block, consisting of trigger signals and machine and beam operation data, and broadcast it over the optical fibre. The event data transmission will be driven by a low-jitter clock derived from the 500 MHz input received from the main RF oscillator. The baseline transmission rate will be 0.5 Gbps, but current provisions allow for an increase of up to 3 Gbps. In repeater mode, the DAMC-X3TIMER rebroadcasts the optical stream from the transmitter to local receivers.

When configured as a receiver, the DAMC-X3TIMER will recover the RF frequency from the input data stream using the clock data recovery (CDR) technique. The recovered clock will be routed to an onboard dual loop clock cleaner which contains two Phase-Locked Loops (PLLs) to reduce the clock jitter and to derive multiple clocks for internal logic and external interfaces. The individual trigger signals and timing data will be extracted from the recovered event data and distributed to local clients via high-speed LVDS/MLVDS links tracing to the MTCA backplane, RTM and AMC's front panel. Coarse and fine programmable delays will be applied to all the output serial links to compensate for differences in optical fibre length resulting from the different positions of the receiver modules along the pre-accelerator chain and the PETRA IV ring.

The DAMC-X3TIMER AMC transmitters and repeaters will also provide drift compensation to keep the propagation delay to the corresponding receivers constant over temperature and humidity changes. For this, each receiver will loop back the data stream to the transmitting/repeating module. A dedicated functional unit on the transmitting/repeating AMC will detect the phase difference between the local reference clock and the clock recovered from the returned data stream. A control loop will configure dedicated delay lines in the receiver and transmitter path to keep the phase relation constant. The measured phase difference and the delay values will be available to the control system for diagnostics. The drift compensation logic will be implemented on a daughter card that will be mounted only on the DAMC-X3TIMER modules performing this function.

The tasks of generating and distributing timing and beam-synchronous signals and data to the PETRA IV subsystems will be assigned to a System-on-a-Chip Field Programmable Gate Array (SoC FPGA) device located on the DAMC-X3TIMER board. The device will be reconfigurable and feature sufficient internal resources to cover the needs of

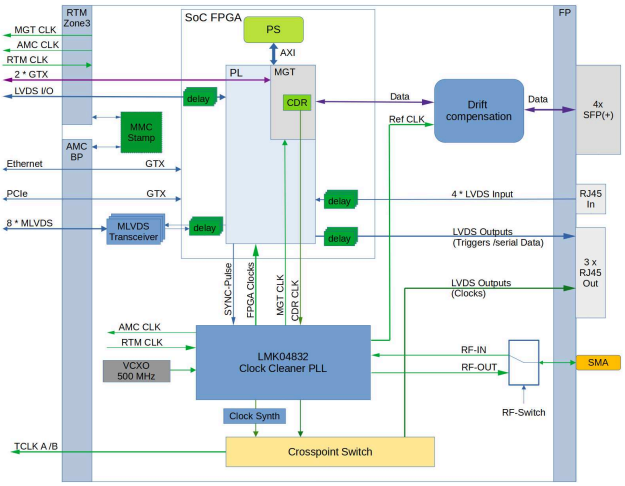

Figure 4: Block diagram of DAMC-X3TIMER prototype.

implementing both the currently foreseen complex real-time processing as well as subsequent upgrades determined by possible enhancements in the timing system's requirements. For configuration, control and monitoring purposes, a PCIe interface will connect the SoC FPGA with the local CPU via the MTCA backplane. The SoC FPGA will distribute the incoming configuration and control data to all internal and onboard programmable locations. In addition, it will collect various status and monitoring data from distributed internal and onboard functional units and provide them on the PCIe bus upon request from the supervising software.

OUTLOOK

The major upgrade of the PETRA storage ring and the pre-accelerator chain requires a new, large-scale, versatile timing system that can deliver precisely and reliably timing information to all the accelerator subsystems and experimental beamlines across the complex. The use of MTCA.4 technology and the vast experience already gained with MTCA.4-based timing systems at the European XFEL and FLASH facilities [4] helps overcome many technological and conceptual hurdles. The DAMC-X3TIMER module, the main functional building block of the timing system, is currently being designed. A fully assembled prototype is expected by the end of 2023. Its functionality will be thoroughly verified in standalone mode in the lab environment and validated in joint tests with other prototypes of the PETRA IV systems.

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