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Current status of the end-of-substructure (EoS) card project for the ATLAS strip tracker upgrade using final ASICs

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Abstract: In the context of the high-luminosity upgrade of the LHC and ATLAS, the microstrip-tracking detector will be redesigned. The main building blocks are substructures with multiple sensors and their electronics. Each substructure will have a single interface to the off-detector system, the so-called End-of-Substructure (EoS) card. Its physical realisation is a set of printed circuit boards (PCBs). The PCB integrates ASICs and hybrids, which multiplex or demultipex the data and transmit with a rate up to 10 Gb/s or receive with a rate up to 2.5 Gb/s on optical fibres. These active parts are developed at CERN and are known as lpGBT and VTRx+. The EoS card integrates the active parts with the required electronics for the specified operation and within the mechanical constraints of the detector. In this paper critical design aspects such as the low-impedance powering scheme and the PCB setup are described. The EoS card has reached its final state for a series production, including the required setups for quality control. The achieved transmission quality on the 10 Gb/s links is presented.

Keywords: Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

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Contents

1 Introduction

The End-of-Substructure (EoS) card is a specialised electronic card, developed for the silicon microstrip detector (ITk-strip) of the ATLAS [1] inner tracker (ITk) [2]. The high-luminosity upgrade of the LHC (HL-LHC) requires a full redesign of the inner tracker and its readout. In section 2, the function and design constraints of the EoS are described. In section 3 the basic design features of the final design are described. In section 4 the results of quality assurance tests to measure the performance of the 10 Gb/s optical upstream link are presented.

2 Design constraints and function of the EoS card

In figure 1, illustrations of the ITk and a single substructure are shown with the positions of the EoS cards indicated. The ITk-strip is built out of 776 substructures. Three different basic geometrical variants of them are needed. At the end of each substructure furthest from the interaction point the EoS collects the electrical signals and connects the power. The EoS is the interface of the modules to the off-detector systems for power, high voltage, control signals and data transfer (figure 2).

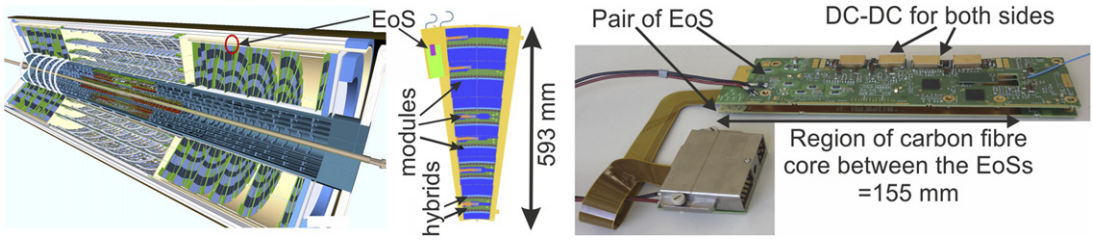

Figure 1. The EoS integrated into the design of the ITK-strip-detector [2] and its own mechanical setup.

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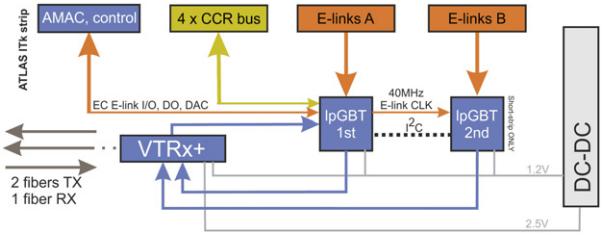

Figure 2. Functional diagram of an EoS in a substructures using the ASICs [5, 6] developed at CERN.

The substructures have central carbon-fibre cores and electrical bus-tapes [3] on each side. Each side is populated with modules [4], which are each a combination of silicon sensor and front-end electronic components mounted on hybrids. The substructures include a protrusion onto which the EoS cards are glued. In figure 1 a photograph of a pair of prototype EoS cards as they will be positioned on either side of the substructure at the protrusion is shown. The carbon fibre core and the DC–DC converters are indicated.

A single EoS represents a single point of failure for all modules on one side of a substructure. Therefore the system design aims to minimise data loss in the case of an EoS failure. No components are shared between the two paired EoS cards of a substructure with the exception of a small number of passive traces that allow slow signals to pass between the pair of EoS cards. These connections allow a single flex-lead connecting to the off-detector systems to service one pair of EoS cards.

Furthermore, the EoS must satisfy strict spatial envelope constraints imposed by the mechanical design of the ITk such as the printed circuit board, PCB, and the mounted components being no thicker than 1.8 mm and 3.2 mm respectively. The connections between the EoS cards allow both 5 mm-thick DC–DC converters to be located on one side of the substructure thereby reducing the overall space envelope.

The fundamental function of the EoS is to be an interface between all modules on one side of a substructure and the off-detector systems. The active components within the EoS card are two radiation hard ASICs developed at CERN known as the low-power Gigabit Transceiver (lpGBT) [5] and the Versatile Link Transceiver (VTRx+) [6]. The modules deliver upstream data at a rate of 640 Mb/s. Each EoS card receives either 14 or 28 such data streams via the eLinks of lpGBTs. They are multiplexed to 10 Gb/s electrical signals by using either one or two lpGBTs. The VTRx+ converts these electrical signals to optical signals (TX) in order to transmit the data to the off-detector systems. Control signals are delivered from the off-detector systems via a receiving fibre (RX, 2.5 Gb/s). The first lpGBT recovers the LHC-clock signal from the RX fibre signal, extracts the control data, and generates control signals for all modules on the side of the substructure. These electrical control signals are sent to the modules as both slow, asynchronous and fast, synchronous signals on Clock, Control, Reject (CCR) buses. Each lpGBT drives 4 CCR buses by using 4 phase-shifting clocks at a frequency of 160 MHz and 8 digital outputs, the aforementioned eLinks.

The functions of all EoS cards are essentially identical. However mechanical constraints within the ITk volume require 14 different physical layouts, known as flavors. The flavors differ in terms of physical layout, number of signals from modules and number of lpGBTs.

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3 Realisation of selected design-aspects

In order to handle the electrical design of the many flavors effectively, the EoS card circuitry is designed in modular blocks. Each block's performance is qualified once. Then the blocks are reused across all flavors with re-assignment of gates and pins as required. The re-assignment allows optimisation of the physical layout. So for all flavors the traces leave the area of the lpGBT well sorted for the other ends of the traces, the bonding pads to the bus tape, see figure 3(a).

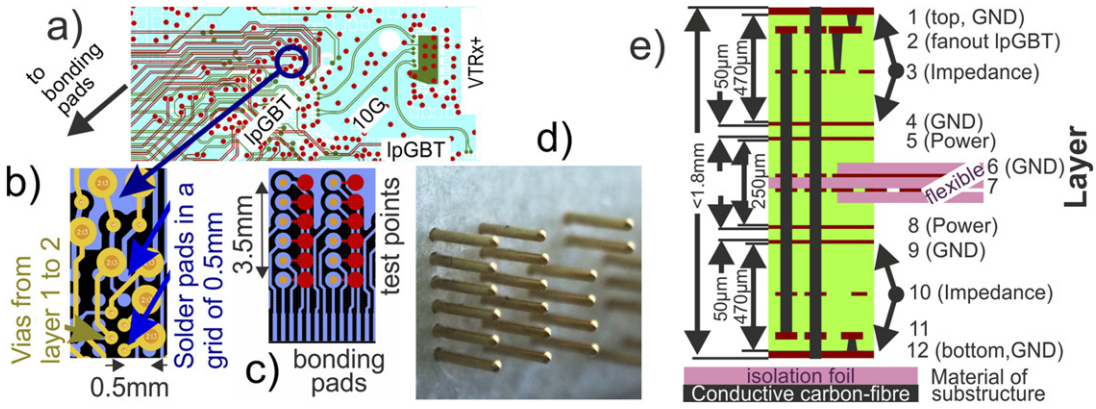

Figure 3. Aspects of the PCB layout details are shown: (a) the differential pairs with minimized crossing: layer 1 (top,GND) blue, 3 (impedance) green, 10 (impedance) red, (b) the lpGBT fan-out with 70 μm structure: layer 1 (top, GND) blue, 2 yellow, (c) test points at bonding pads: layer 1 (top, GND) blue, 12 (bottom, GND) red, (d) detail of the needle prober to touch the bottom test points in a pitch of 0.7 mm and (e) cross section view of the layer stack of the PCB.

The footprint of the lpGBT is a dense 0.5 mm ball grid area (BGA) with an area of 9×9 mm^2. The most challenging aspect of the PCB manufacturing is the combination of the lpGBT fan-out area with other PCB requirements. Moreover, the EoS is large (≈25 cm) and requires a semi-rigid setup, a 12-layer PCB, halogen-free materials and sufficient copper grown into the vias. Overall, the total quantity of 2000 EoS cards, distributed over 14 different flavors, is disfavoured by manufacturers for complex PCBs. These challenges have led to a vendor-specific design. The PCB is kept in an industrial standard 100 µm technology with the exception of the small areas around the lpGBT chips. In the two top layers 70 µm structures are used to pass traces between the solder balls of the BGA and for vias between the top layer 1 and the first inner layer 2 (figure 3(b)).

A symmetrical layer stack around the central layer is advisable to keep the PCBs flat (figure 3(e)). The needed 46 differential pairs and inevitable crossings require two impedance controlled layers (100 Ω). These layers must be inner layers with thick insulators and located between GND-planes, because the bottom layer is glued to a conductive carbon-fibre core. Nevertheless the total thickness of the PCB must be kept below 1.8 mm. Hence the fan-out layer 2 is integrated into the insulation material of the impedance controlled structure. A central, double sided, flexible layer contributes another 250 µm to the thickness. In addition two power planes are required. All these features are combined into a PCB with 12 layers.

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The 10 Gb/s links and sub-nanosecond rise times in the neighbourhood of sensitive silicon strip sensors require a planned powering scheme. Even though only two different voltages (2.5 V and 1.2 V) are required, 7 different power domains are foreseen by the ASIC-designs. In figure 4(a) schematic of the powering circuit is provided. The air coils indicated in figure 4 provide only a small decoupling from the DC–DC converters to the domains and between the different domains. The choice of air coils is constrained by the 2 T magnetic field within the ITk [1] and the 3.2 mm limit on all component heights. Each domain has its own set of buffering capacitors. The concept [7, 8] of combining nearby power-ground layers of thickness 50 µm for high frequencies (>100 MHz) with different discrete ceramic capacitors is used, with resistors added to damp triggered spikes. Approximations in PSPICE/VHDL-AMS simulations with realistic models show that the impedance is below 0.1 Ω for a wide frequency range (100 kHz to 300 MHz). The phase between voltage and current is not 90°. Therefore spikes are damped. The low impedance, the phase and the planar structures allow to place the capacitors away from the consumer. This freedom is used to keep the area of the PCB, which is glued to the carbon-fibre structure, free of components (see figure 1).

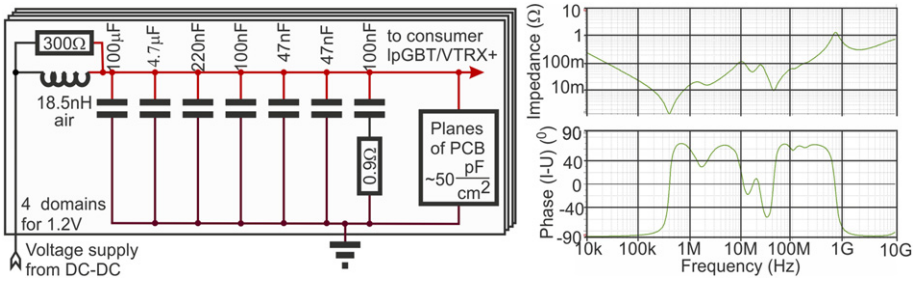

Figure 4. On the left a schematic of the power circuit is shown. On the right the result of a simulation to characterize the impedance of the circuit is shown with impedance and phase plotted against frequency.

4 Design check and quality control for the optical up-link

For the quality control (QC) of all cards, test points are designed onto the EoS cards within 5 mm distance to the bonding pads. The ones on the bottom side of the PCB, will be contacted with a specially designed bed of spring loaded needles on a grid of 0.7 mm, see figures 3(c) and (d). Fast signals of 640 Mb/s can be injected through the needles simultaneously without touching the sensitive bond-pads. This allows all of the traces to be checked electrically, except for the very last millimeters.

The most critical contributors for the performance of the EoS are the 10 Gb/s links. The baseline for the expected data-transmission performance is set by the design specifications of the lpGBT and VTRx+ with some degradation expected from the PCB and associated design constraints. To confirm the performance of the EoS card, eye diagrams are recorded using an optical sampling scope, (see figure 5). The measured individual samples are compared to a mask

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defined by the VTRx+ developers [10]. For the nominal operational settings of the lpGBT and VTRx+ no violations of the mask are observed. The estimated probabilities of bit errors are far below the maximum permissible rate of 10^{-12}. No significant dependence of the eyes to the environmental temperature (−40 °C to +20 °C) was observed. That range covers the expected operation conditions for the ITk-strip-detector.

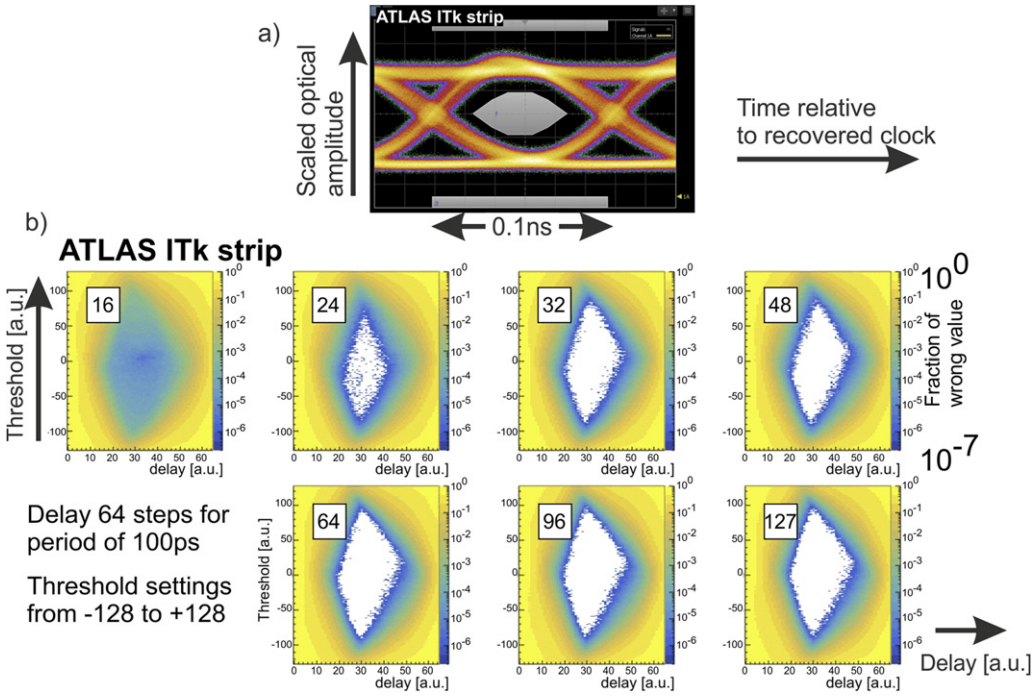

Figure 5. Eye diagrams for a typical optical link: (a) measured with an optical sampling scope (bandwidth ≈ 7.5 GHz). (b) Scanned within the receiving FPGA—the parameter is the TX-amplitude of the lpGBT.

These measurements require complex equipment and thus cannot be performed on each EoS card of the serial production. Therefore a VHDL-code for the KC705-board [9] was developed. The IP-core, which the FPGA-vendor provides, is adapted to an ASIC-FPGA data-stream. Delays and thresholds are scanned at the receiving port of the FPGA. Resultant readings are compared to the unaltered signal with mismatched logic states counted as errors. In figure 5 good and bad eye diagrams are shown. For this test the quality of the data transfer is changed by reducing the modulation current at the driver for the TX-signal within the lpGBT. It is linear to a digital parameter from 0 to 127. The highest current, 127 ≙ 17.4 mA, is the default for the version 1 of the lpGBT. For each scanned point a sensitivity of 10^{-7} errors per transferred bits is reached with a measurement time of 10 minutes for the total scan. These tests will run in parallel with all of the other tests at both cold and room temperatures. A set of thresholds that will define an acceptable eye-diagram in the quality control campaign is yet to be defined.

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5 Summary and outlook

The designs for 10 of the required 14 flavors are ready and behave well in all tests without requiring further debugging. The production times and prototype turn-around times suffer from the none industrial standard designs. Around 30 EoS cards are used in system tests of the substructures [11] and no limitations of the system performances are traced to the EoS-design. The next steps are preparing the production, tuning the quality control with statistic of produced boards. The design work for the last flavors requires modifications in the geometry of the flex-leads only.

Acknowledgments

We thank the ITk and ATLAS collaborations for letting us take part in the interesting development.

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