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Current status of the End-of-Substructure (EoS) card project for the ATLAS Strip Tracker Upgrade using final ASICs

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Abstract: The silicon tracker of the ATLAS experiment will be upgraded for the upcoming High-Luminosity Upgrade of the LHC (HL-LHC). The main building blocks of the new strip tracker are modules that consist of silicon sensors and hybrid PCBs hosting the read-out ASICs. The modules are mounted on rigid carbon-fibre substructures, that provide common services to all the modules. At the end of each substructure, a so-called End-of-Substructure (EoS) card facilitates the transfer of data, power, high voltage and control signals between the modules and the off-detector systems. The module front-end electronics transfer data to the EoS card on 640 Mbit/s differential lines. The EoS connects up to 28 data lines to one or two lpGBT chips that provide data serialisation and uses a 10 GBit/s versatile optical link (VTRx+) to transmit signals to the off-detector systems. The lpGBT also recovers the LHC clock on the down-link and generates clock and control signals for the modules. To meet the tight integration requirements in the detector, several different EoS card designs are needed. Production-ready EoS card's electronic design integrating final lpGBTv1 and VTRx+ ASICs from CERN are described, as well as results from recent quality assurance tests including detailed characterisation of the opto-electronics system by its bit error rate, jitter, and eye diagram representation. Since each EoS sits at a single-point-of-failure for an entire side of a substructure, a dedicated quality control (QC) procedure for the production has been developed.

Keywords: Electronic detector readout concepts (solid-state), Front-end electronics for detector readout

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Contents

1 Introduction

The End-of-Substructure (EoS) card is a special electronic card, developed for the Si-strip detector of the ATLAS [1] inner tracker (ITk) [2]. The high-luminosity upgrade of the LHC requires a full redesign of the inner tracker and its readout. The following sections will describe the task and the constraints for the EoS, given by the general concept of the inner tracker, the basic design features, applied to reach the performance, and the performance of the 10 Gbit/s upstream link, as an important example of the design checks and of the quality control.

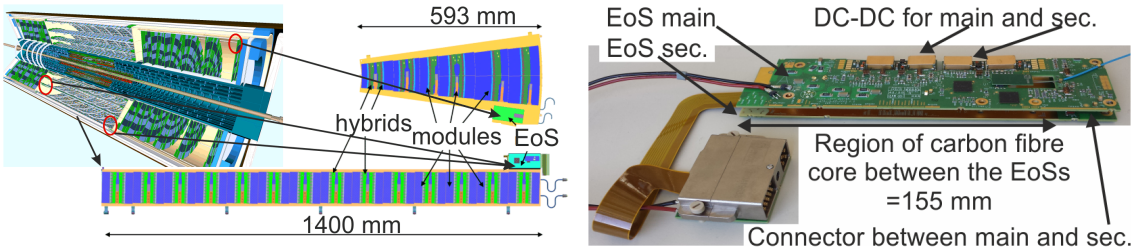

Figure 1. The EoS integrated into the design of the ITK-strip-detector [2] and its own mechanical setup.

2 Task of the EoS and constrains by the ITK concept

The strip detector, figure 1, detects the particles with 4 nearly cylindrical layers in the central barrel region. The end-caps consist of 6 disks each. These are built out of substructures: 392 staves for the barrel and 384 petals for the end-caps. At the end of each substructure farthest away from the interaction point the EoS collects the electrical signals and connects the power. The EoS is the interface of the modules to the Off-detector systems for power, high voltage and signals.

The substructures have central carbon-fibre cores and electrical bus-tapes [3] on each side. Each side is populated with modules [4], a combination of silicon detectors and electronic-hybrids. The carbon-fibre core continues into an ear. A pair of EoS cards are glued onto the ear with their

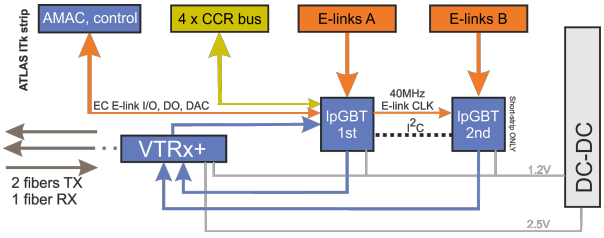

Figure 2. Functional diagram of an EoS in a substructures using the ASICs [5, 6] developed at CERN.

rigid parts, one on each side of the carbon-fibre core. Bus-tapes and EoS will be connected by wire bonding.

Because the EoS is located inside the tracking volume, it has to satisfy the constraints defined by the mechanical design. For one of the paired EoS cards, a connector to the Off-detector systems is soldered onto another rigid part. It is used for a small set of control signals, high voltage and power input. It will be located on the general support of the ITk-subsystem away from the substructure. A flex-lead, integrated into the PCB, connects signals with low currents between the two rigid parts. Paired wires are used for supply and return currents (<10A). The total height of a populated PCB has to be smaller than 5 mm. The design is sharing that between the (<1.8 mm) PCB and components (<3.2 mm). All tall components, specially the DC-DCs for supply, are kept on one side. That PCB is called "Main", while the other even thinner is called "Secondary", or "Sec.". Both PCBs handle the signals of its own side of the substructure only. By that each PCB is a single point of failure for just one side. To keep that limited to one side the partner PCB has just passive traces for the other side, but no common components. That keeps the risk of loosing a whole substructure low. The interconnect is provided by a standard connector in the region without carbon-fiber core. That connection is needed, because space is available for one common connector only and both DC-DC are located on the main side.

The task of the EoS is the interface between the modules and the Off-detector systems. The active parts are the radiation hard chip-set developed at CERN. The modules deliver per side of the substructure 14 or 28 electrical links upstream data, each at 640 Mbits/s. They are multiplexed to 10 Gbits/s electrical signals by using either one or two lpGBTs [5]. The VTRx+ [6] converts these electrical signal to optical signals (TX) , which transmits the data to the Off-detector systems. On a receiving fibre (RX, 2.5 Gbits/s) control signals are delivered. From the RX, the LHC-clock is recovered and the control signals are sent to the modules as slow asynchronous data and fast synchronous CCR-buses - Clock, Control, Reject. 4 CCR-buses are generated by 4 phase shifting 160 MHz clocks and 8 ELINK-outs.

The ADCs of the first lpGBT are used mainly for monitoring. A requirement for accuracy (10 bit) appears as ratio between two channels only. With them the DAC is compared to the sense voltage of the external power supply. That allows for the cross calibration of the modules, receiving the DAC, against the Off-detector reference seeing the sense. All the control is realized in the first lpGBT, because the second is not always populated and has no access to the fast information provided by the optical RX-fibre. That used up the features of the lpBGT in the configuration for 640 Mbit/s.

The realization of the EoS as main and secondary, differences in the geometry of the barrel

and of the end-caps, and in addition radial dependent differences for the barrel 14 different designs of the EoS are needed, called flavors. They differ in geometry, number of signals from the modules to handle and number of populated lpGBTs.

3 Basic design features

In order to handle the many flavors effectively and to be prepared for common updates requested by parallel ongoing developments, hierarchical designs have been setup for the circuit diagrams. The flavor dependent top-levels are connecting blocks differently, which are commonly designed for all flavors. The bottom blocks are configurable per hierarchical appearance in choosing a specific chip (e.g. lpGBT-1, lpGBT-2), in specific pins and gates, in decision for leaving components unpopulated or in changing of their values and footprints. As a result, a block manufactured and tested in one flavor or changed for updates was proven for the other flavors as well. The gate swap option per hierarchical appearance was used, to optimize the connection of the lpGBTs to the bonding pads for minimal space and number of vias, see figure 3a. To take any risk of performance degradation from the 10 Gbits/s traces away, that technique helped to route all the other differential traces on just two impedance controlled layers limited by the requirement of PCB thickness (<1. 8mm) . The performance of the 10 G-traces, see later in section 4, was not verifiably improved by taking the crossing traces away, but the effort removed all questions and might provide head-room on a system level. They are likely limited by other factors or even by the measurement itself.

A critical issue for the production of the PCBs is the fan-out area of the 0.5 mm ball grid (BGA) of the lpGBT in combination with the large sizes of the PCBs (25cm), the semi-rigid setup, a 12 layer PCB, a reasonable total quantity of 2000 pieces, yet distributed over 14 flavors, and finally also the restriction to halogen free materials. This lead to a vendor-specific design. The main part of the PCB is kept in an industrial standard of 100 μm technology. Only for the two top layers, and within those only in the areas of the lpGBT chips of a size of 9× 9 mm^2 that rule is violated and 70 μm structures are used (figure 3).

A symmetrical layer stack around the central layer is advisable to keep the PCBs flat. The needed 46 differential pairs and inevitable crossings require two impedance controlled layers (100 Ω). These have to be inner layers, because the bottom layer is glued to a conductive carbon-fibre core. By integrating the fan-out layer for the lpGBT into the insulation material of the impedance controlled

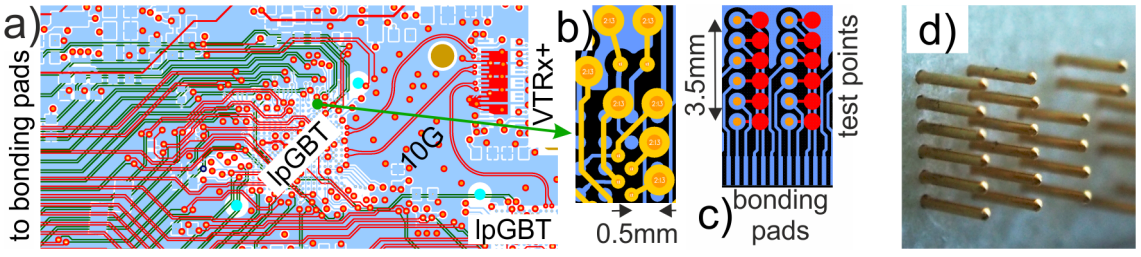

Figure 3. Layout details: **a)** The differential pairs with minimized crossing: Layer 1 (top,GND) blue, 3 (impedance) red, 10 (impedance) green, **b)** Fan-out with 70 μm structure : Layer 1 (top, GND) blue, 2 yellow, **c)** Test points at bonding pads: Layer 1 (top, GND) blue, 12 (Bottom, GND) red and **d)** Detail of the needle prober to touch the bottom test points in a pitch of 0.7 mm .

structure it was possible to limit the total thickness of the PCB, however at the cost of not being able to use that layer freely near impedance controlled traces. On the inner layers each structure of type GND-trace-GND requires a thickness of 470 μm using 100 μm wide traces. Together with a central double sided flexible layer and layers for GND and power a 12 layer PCB is designed and the manufacturer adds two layers for technical reasons.

10 Gbits/s links and rise times below 1 ns in the neighborhood of sensitive silicon strip sensors enforced a planned powering scheme. Even though only two different voltages (2.5 V and 1.2 V) are required, 7 different power domains are foreseen by the ASIC-designs. They are decoupled by small (1.8 nH) air coils and parallel 300 Ω resistors. The decoupling strength is limited by the ATLAS central magnetic field of 2 T [1], the limit of component height (3.2 mm) and space on the PCB. Each domain has its own set of decoupling capacitors. The concept [7, 8] of combining nearby power-ground layers (50 μm, ≈50 pF/cm^2) for high frequencies (>100 MHz) with different discrete ceramic capacitors as well as an RC combination (100 nF, 0.9 Ω) is used. Approximations in PSPICE/VHDL-AMS simulations with realistic models show that the impedance is below 0.1 Ω for a wide frequency range (100 kHz to 30 MHz) and the phase between voltage and current damps triggered spikes partially. This realisation allows to place the capacitors away from the consumer. Not soldering the capacitor onto the bottom side opposite to the consumers keeps the bottom side of the PCB flat, which is important for the gluing to the carbon-fibre core. A 4 mm wide gap around the lpGBTs allows for optical inspection of the BGA soldering during the quality control(QC).

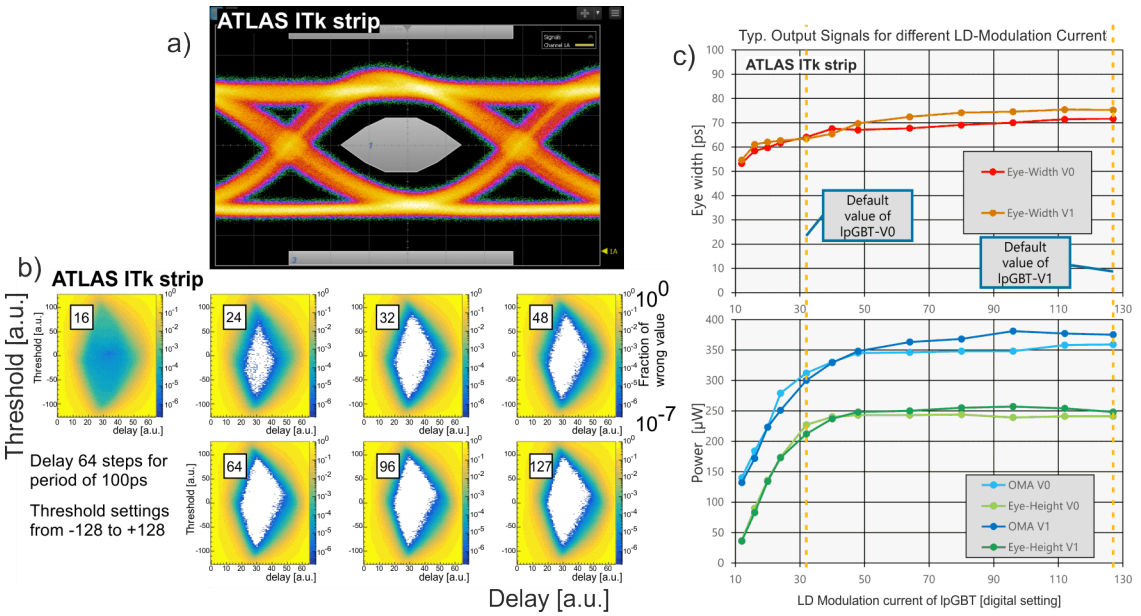

Figure 4. Eye diagrams for a typical optical link: **a)** Measured with an optical sampling scope (bandwidth ≈7.5 GHz). **b)** Generated by a scan within the receiving FPGA and **c)** Parameters of the eye in a) versus the setting of the amplitude of the lpGBT output driver. In b) the parameter is that setting. The mask in a) is taken from the ASIC-designers [10].

4 Design check and quality control for the optical up-link

For the quality control (QC) of all cards, test points are designed onto the EoS cards within 5 mm distance to the bonding pads. The ones on the bottom side of the PCB, will be contacted with a specially designed bed of spring loaded needles on a grid of 0.7 mm, see figure 3. Fast signals of 640 Mbits/s can be injected without touching the sensitive bond-pads. This allows all of the traces to be checked electrically, except for the very last millimeters, which are checked optically and electrically during PCB-production.

The most critical contributors for the performance are the 10 Gbits/s links. The designs are checked with an optical sampling scope with an analog bandwidth of ≈7.5 GHz (see figure 4). After observing that with default settings the version 0 and 1 of the lpGBT behave differently, scans of the 10 Gbit/s signals over the programmable output amplitudes of the lpGBT were performed. The defaults of the respective parameter are different for the two available chip versions, V0 and V1. A slight dependence of the eye width and height on that parameter was observed (figure 4). Setting it to the maximum modulation the best performance is reached and the ASIC designers do not expect drawbacks. No significant dependence to the environmental temperature (-40^{0}C to +20^{0}C) was observed. That range covers the expected operation conditions for the ITk-strip-detector.

These measurements require too complex equipment and thus cannot be performed on each EoS card of the serial production. Therefore a VHDL-code for the KC705-board [9] was developed not relying on a special protocol. Within the receiving port of the FPGA a delay and threshold is set and wrong readings compared to the good timing are counted. In figure 4 good and bad eye diagrams are shown by scanning the modulation amplitude of the output of the lpGBT. Within 10 minutes fractions of 10^{-7} per bin are detected. These tests will run in parallel with all of the other tests at both cold and room temperatures. A parameterisation for good and bad eye diagrams during an automated test has yet to be developed.

5 Summary and outlook

The designs for 10 of the required 14 flavors are ready and behave well without debugging in all the tests. The production times and prototype turn-around times suffer from the none industrial standard designs. Around 30 EoS cards are used in system tests of the substructures [11] and no limitations of the system performances are traced to the EoS-design. The next steps are preparing the production, tuning the quality control with statistic of produced boards. The design work for the last flavors requires modifications in the geometry of the flex-leads only.

Acknowledgments

We thank the ITk and ATLAS collaborations for letting us take part of the interesting development.

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