Development of CoRDIA: an Imaging Detector for next-generation Synchrotron Rings and Free Electron Lasers

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Abstract. An X-ray imager is being developed for use in diffraction-limited Synchrotron Rings and Continuous Wave Free Electron Lasers. The imager is named CoRDIA (COntinuous Readout Digitising Imager Array) and aims at achieving continuous operation at a frame rate in excess of 100kHz. Other goals include single-photon sensitivity at 12 keV (or below), a full well in excess of 10k photon/pixel/image, and a 100µm pixel pitch. The detector ASIC will be compatible with multiple sensor materials to cover different energy ranges. Exploratory prototypes of the readout ASIC (basic circuital blocks) have been manufactured in in TSMC 65nm technology: they are presenltly under test.

1 Introduction

Most of imaging detectors available for Photon Science experiments today can be rougly be divided between the ones capable of continuous operation at moderate speed -i.e. capable of readout at rate up to a few k-frame/s, and often used in Synchrotron Rings (SRs) and low-repetition-rate Free Electron Lasers (FELs)- and the ones optimized for high-repetition-rate Free Electron Lasers -capable of a few M-frame/s, but only for short imaging bursts-.
Both the upgrading of SRs to diffraction-limited operation (expected to increase brilliance by two orders of magnitude), and the shift of fast FEL sources from pulsed to Continuous Wave operation (which will marginally reduce the peak readout rate requirement, but would make continuous readout a must), points out the common need for bridging the gap between the two categories of detectors, and to provide imaging detectors able to operate continuously at a frame rate in excess of 100k frame/s.

2 CoRDIA development

A collaboration between DESY and Bonn University is developing an instrument to fill this need: the CoRDIA detector (COntinuous Readout Digitising Imager Array).
Our goals include continuous operation between 100 and 200 kframe/s, single-photon sensitivity at 12 keV (or below), a full well in excess of 10k photon/pixel/image, and a 100µm pixel pitch.

The detector system is foreseen to be built up as a multi-module array of hybrid assembles, including a common readout ASIC compatible with multiple sensor materials: p-doped Silicon for the main (10 keV) energy range, high-Z materials for higher energies, and sensors with built-in amplification for soft X-rays.
The readout ASIC adopts a continuous writing-reading scheme, based on a pipelined signal process-chain, so that while one image is being integrated, the previous image is digitized by on-pixel ADCs, and the image before that is streamed out through a fast readout system.
For the analog front end we use an adaptive-gain charge-integrating block, able to adjust the system gain to the incoming photon flux. We plan to use a modular "superpixel" structure, with multiple analog front ends feeding a circuit for Correlated-Double-Sampling and being digitized by an ADC. The ADCs are based on successive approximation architecture, and are distributed in the pixel array. For the digital streamout, we plan to adopt the principle of the GigabitWireTransmitter solution developed by Nikhef for Timepix4.
An overview of the pipeline achitecture is presented in Figure 1.

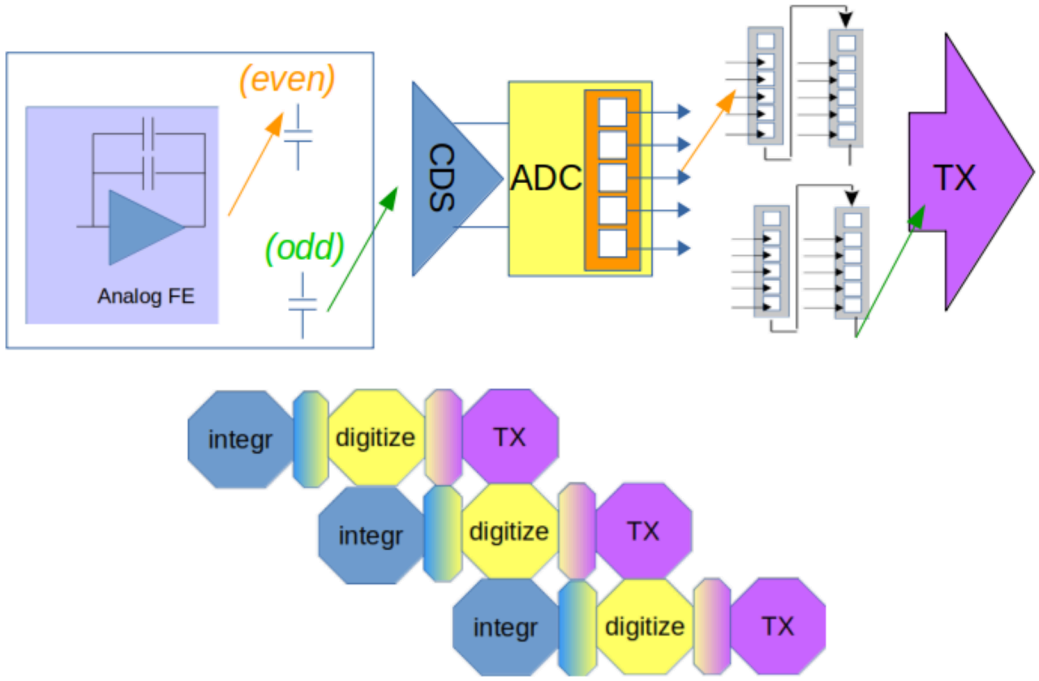

Figure 1. CoRDIA pipeline architecture.

Exploratory prototypes of the readout ASIC basic circuital blocks (Figure 2) have been designed in TSMC65nm technology and have been manufactured in an MPW.
Circuital solutions have been included to validate the charge-integrating block (built on the experience of the AGIPD detector for the Eu.XFEL), a Correlated Double Sampling stage (to reduce noise), and the pipelined architecture (to achieve continuous operation at the target frame rate). Four ADC variants have been included, to explore redundancy and advanced-switching options.
Our present goal is to test indvidual components to verify that each stage of our pipleline is not a critical bottleneck for our frame rate aims: preliminary tests suggest that a continuous frame rate in excess of 150kHz would be achieveable.

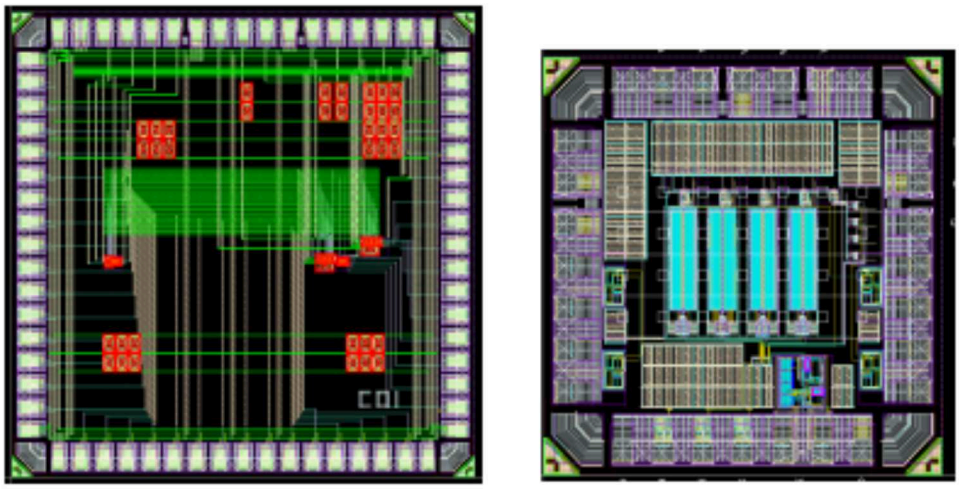

Figure 2. CoRDIA basic circuital block prototypes.
Left: front-end analog circuits. Right: ADC vatiants

After test and validation of single circuital blocks, we plan to follow a gradual approach (Figure 3), first developing a 1st-generation ASIC that, while usable for scientific experiments, will have moderate performances (targeting mainly pixel pitch, continuous readout operation and frame rate). Our aim is to have this first version available by DESY's Petra IV start of operation, about 2027.
The 1st-generation ASIC will be followed by a 2nd-generation ASIC, that will correct eventual bugs and aim at extending dynamic range, reducing noise, and minimizing blind areas.

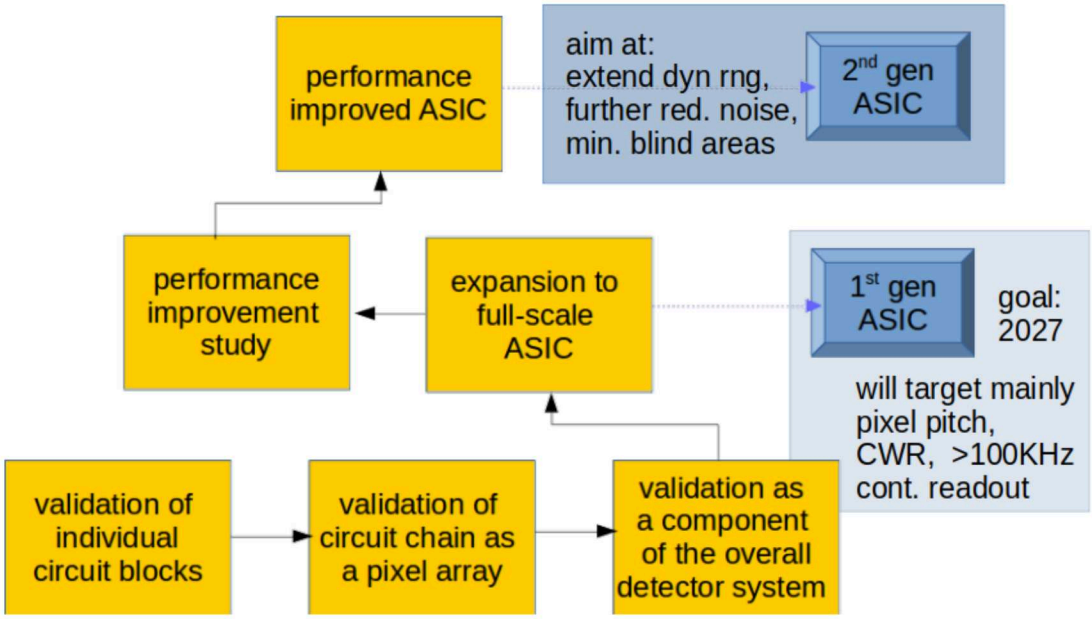

Figure 3. CoRDIA overall project plan.

Even for an array of just 1Mpixel and for a reduced frame rate at the bottom of our range (100k frame/s), the detector is foreseen to produce a signficative data output, of the order of 1.4 Tb/s. For our goal frame rate of 150k frame/s, and considering some overhead coming from data padding and encoding, the throughput might easily get over 2Tb/s.

We plan to address the issue both on-Silicon (by means of on-chip digitization through parallel ADCs and high speed drivers), and out-of-Silicon (by using high-performance FPGAs to serialize the data, and high-speed optical links). Hardware acceleration solutions for image correction and conventional compression methods are under consideration, as well as data reduction schemes on preprocessing hardware, to reduce the data volume arriving to later processing stages.