Development of CoRDIA: an Imaging Detector for next-generation Synchrotron Rings and Free Electron Lasers

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Development of CoRDIA: an Imaging Detector for next-generation Synchrotron Rings and Free Electron Lasers

A Marras[1], A Klujev[1], S Lange[1], T Laurus[1], D Pennicard[1], U Trunk[1], C B Wunderer[1], M L Hafiane[2], T Hemperek[2], T Kamilaris[2], H Krueger[2], T Wang[2] and H Graafsma[1,3]

1) Center for Free-Electron Laser Science CFEL, Deutsches Elektronen-Synchrotron DESY, Germany
2) University of Bonn, Bonn, Germany
3) Mid Sweden University, Sundsvall, Sweden

corresponding author: alessandro.marras@desy.de

Abstract. An x-ray imager is being developed for use in diffraction-limited synchrotron rings and continuous wave free electron lasers. The imager is named CoRDIA (COntinuous Readout Digitising Imager Array) and aims at achieving continuous operation at a frame rate in excess of 100kHz. Other goals include single-photon sensitivity at 12 keV (or below), a full well in excess of 10k photon/pixel/image, and a 100µm pixel pitch. The detector ASIC will be compatible with multiple sensor materials to cover different energy ranges. Exploratory prototypes of the readout ASIC (basic circuital blocks) have been manufactured in TSMC 65nm technology: they are presently under test.

1 Introduction

Most of imaging detectors available for photon science experiments today can be roughly divided between the ones capable of continuous operation at moderate speed, i.e. capable of readout at rate up to a few k-frame/s [1,2], often used at synchrotron rings (SRs) and low-repetition-rate free electron lasers (FELs), and the ones optimized for high-repetition-rate FELs, capable of a few M-frame/s, but only for short imaging bursts [3,4,5].

Both the upgrading of SRs to diffraction-limited operation (expected to increase brilliance by two orders of magnitude), and the shift of fast FEL sources from pulsed to continuous wave (CW) operation (which will marginally reduce the peak readout rate requirement, but would make continuous readout a must), points out the common need for bridging the gap between the two categories of detectors, and to provide imaging detectors able to operate continuously at a frame rate in excess of 100k frame/s.

2 CoRDIA development

A collaboration between DESY and Bonn University is developing an instrument to fill this need: the CoRDIA detector (COntinuous Readout Digitising Imager Array).

Our goals include continuous operation between 100 and 200 kframe/s, single-photon sensitivity at 12 keV (or below), a full well in excess of 10k photon/pixel/image, and a 100µm pixel pitch.

The detector system will be built up as a multi-module array of hybrid assembles, including a common readout ASIC compatible with multiple sensor materials: p-doped Silicon for the main (10 keV) energy range, high-Z materials for higher energies, and sensors with built-in amplification for soft X-rays (below 3keV).

The ASIC uses a continuous writing-reading (CWR) approach based on a pipelined signal processing chain, so that while one image is being integrated, the previous image is digitized by on-chip ADCs, and the image before that is streamed out through a fast driver.

For the analog front end, we have designed an adaptive-gain charge-integrating block inspired by the AGIPD detector [6], able to adjust the system gain to the incoming photon flux.

Similarly, a correlated-double-sampling (CDS) circuit hs been designed to reduce noise.

We have designed an ADC using a successive approximation architecture with reduced size, so that it can be integrated in a modular "superpixel" structure within the pixel array. Digitization speed has been defined so that multiple (16) analog front ends can feed feeding sequentially a circuit for a CDS and being digitized by an ADC without hampering the frame rate.

For the digital readout, we plan to adopt the principle of the gigabit wire transmitter (GWT) solution developed by NIKHEF for Timepix4 [7]. While we have not yet redesigned this block yet, we reached an agreement for the the reuse of the NIKHEF-developed layout.

An overview of proposed the pipeline achitecture is presented in Figure 1.

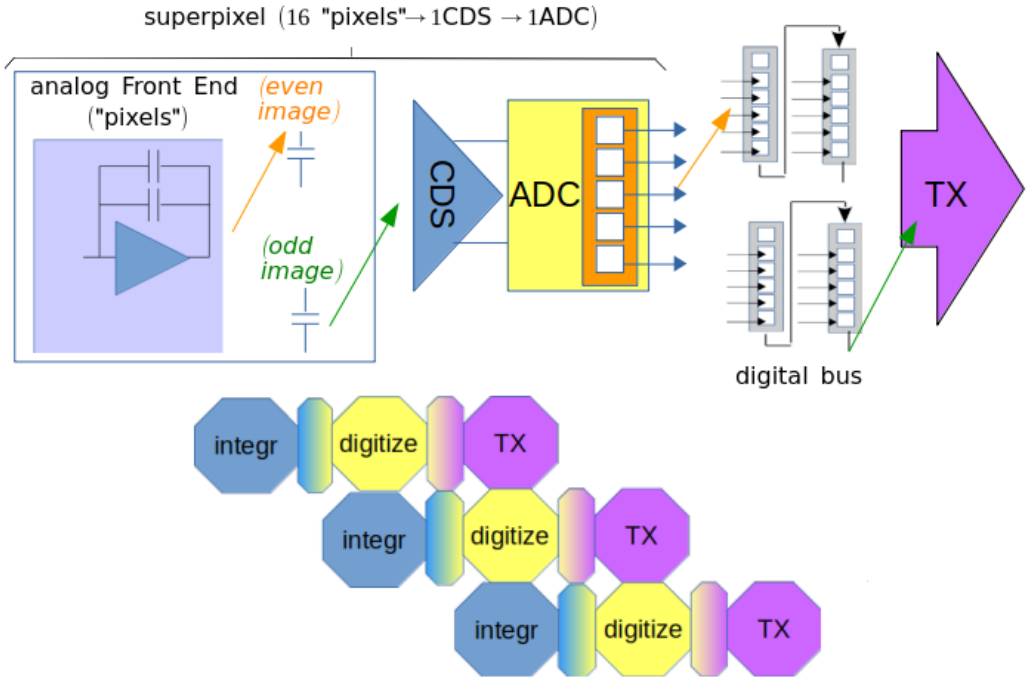

Figure 1. CoRDIA pipeline architecture. While an image is being integrated by the preamplifier into a capacitor, the former image is retrieved by a second capacitor and passed to the Correlated-Double-Sampling (CDS) and ADC circuit. Similarly, while an image is being digitized, the image before is sent out through the transmitter (TX) block. The signal path alternates for even (orange) and odd (green) images in a "ping-pong" fashion, allowing continuous Continuous Writing-Reading (CWR)

Exploratory prototypes (Figure 2) of the readout ASIC basic circuit blocks have been designed in TSMC 65nm technology and have been manufactured in an Multi Project Wafer (MPW), also using IPs provided b CERN and by the RD53 collaboration.

Circuit solutions have been included in the MPW to validate the charge-integrating block and the Correlated Double Sampling stage, both as isolated blocks and as pipelined stages. Four ADC variants have been included, to explore redundancy and advanced-switching options in the digitization process. The circuits are presently under test.

Our present goal is to test indvidual components to verify that each stage of our pipleline is not a critical bottleneck for our frame rate aims: preliminary tests suggest that a continuous frame rate in excess of 150kHz would be achieveable. Details of the test results will follow in future publications.

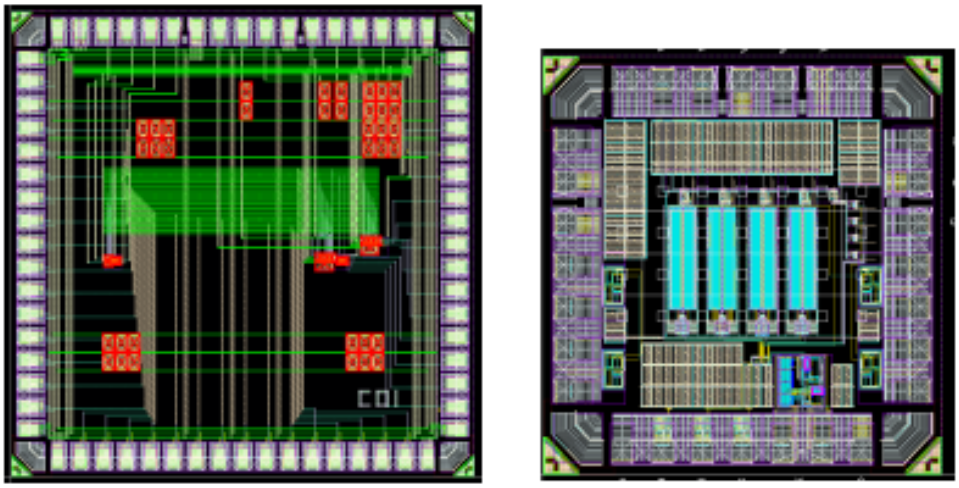

Figure 2. CoRDIA basic circuit block prototypes.
Left: front-end analog circuits. Right: ADC variants

After test and validation of single circuit blocks, we plan to follow a gradual approach (Figure 3), first developing a 1st-generation ASIC that, while usable for scientific experiments, will achieve only some of our goals (targeting mainly pixel pitch, continuous writing-reading operation and frame rate). Our aim is to have this first version available by DESY's PETRA IV start of operation, about 2027.

The 1st-generation ASIC will be followed by a 2nd-generation ASIC, that will correct eventual bugs and aim at extending dynamic range, reducing noise, and minimizing blind areas.

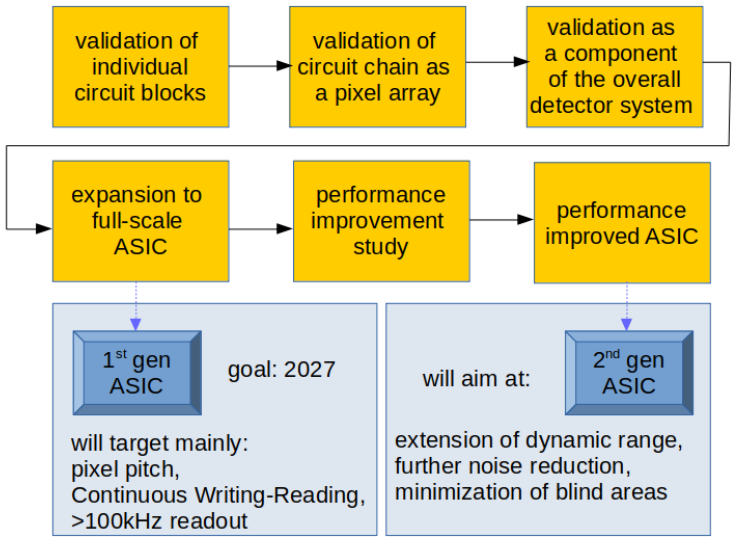

Figure 3. CoRDIA overall project plan.

Even for an array of just 1Mpixel and for a reduced frame rate at the bottom of our range (100k frame/s), the detector is foreseen to produce a signficative data output, of the order of 1.4 Tb/s. For our goal frame rate of 150k frame/s, and considering some overhead coming from data padding and encoding, the throughput might easily get over 2Tb/s.

We plan to address the issue both on-Silicon (by means of on-chip digitization through parallel ADCs, as a digital streamout allows the use of high speed drivers, like the chosen GWT), and out-of-Silicon (by using high-performance FPGAs to serialize the data, and high-speed optical links). Hardware acceleration solutions for image correction and conventional compression methods are under consideration, as well as data reduction schemes on preprocessing hardware, to reduce the data volume arriving to later processing stages.

3 Conclusions

An X-Ray Imager is being developed, for diffraction-limited synchrotron rings and continuous wave free electron lasers.

Its main feature is being capable of continuous image acquisition at high frame rate (>100kHz). The general architecture has been defined, and basic circuital blocks have been designed and manufactured in an MPW they are presently under test.

We aim for the first generation of the detector to be usable by the start of operation of the diffraction-limited upgrade of DESY storage ring (Petra IV), about 2027.

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