

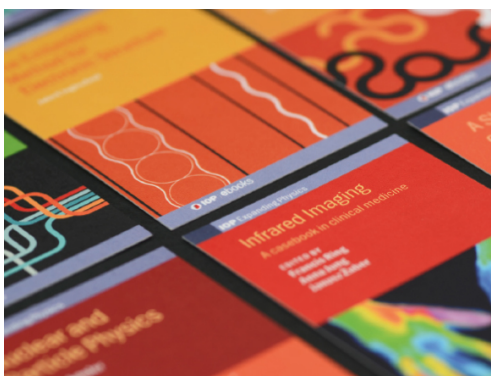
Mini-MALTA: radiation hard pixel designs for small-electrode monolithic CMOS sensors for the High Luminosity LHC

To cite this article: M. Dyndal *et al* 2020 *JINST* **15** P02005

View the [article online](#) for updates and enhancements.

Recent citations

- [Charge collection properties of TowerJazz 180 nm CMOS Pixel Sensors in dependence of pixel geometries and bias parameters, studied using a dedicated test-vehicle: The Investigator chip](#)
G. Aglieri Rinella *et al*
- [New method for estimating detector efficiency for charged particles with Diamond Light Source](#)
K. Metodiev *et al*
- [DMAPS Monopix developments in large and small electrode designs](#)
C. Bospin *et al*



IOP | ebooks™

Bringing together innovative digital publishing with leading authors from the global scientific community.

Start exploring the collection—download the first chapter of every title for free.

RECEIVED: September 20, 2019

REVISED: December 13, 2019

ACCEPTED: January 19, 2020

PUBLISHED: February 10, 2020

Mini-MALTA: radiation hard pixel designs for small-electrode monolithic CMOS sensors for the High Luminosity LHC

M. Dyndal,^a V. Dao,^a P. Allport,ⁱ I. Asensi Tortajada,^{a,b} M. Barbero,^m S. Bhat,^m D. Bortoletto,^c I. Berdalovic,^{a,j} C. Bepin,^k C. Buttar,^f I. Caicedo,^k R. Cardella,^{a,d} F. Dachs,^{a,e} Y. Degerli,ⁿ H. Denizli,^l L. Flores Sanz de Acedo,^{a,f} P. Freeman,ⁱ L. Gonella,ⁱ A. Habib,^m T. Hemperek,^k T. Hirono,^k B. Hiti,^g T. Kugathasan,^a I. Mandić,^g D. Maneuski,^f M. Mikuž,^g K. Moustakas,^k M. Munker,^a K.Y. Oyulmaz,^l P. Pangaud,^m H. Pernegger,^{a,1} F. Piro,^a P. Riedler,^a H. Sandaker,^d E.J. Schioppa,^a P. Schwemling,ⁿ A. Sharma,^{a,c} L. Simon Argemi,^f C. Solans Sanchez,^a W. Snoeys,^a T. Suligoj,^j T. Wang,^k N. Wermes^k and S. Worm^{i,o}

^aCERN, Geneva, Switzerland

^bUniversity of Valencia and Consejo Superior de Investigaci Científicas (CSIC), Valencia, Spain

^cUniversity of Oxford, Oxford, U.K.

^dUniversity of Oslo, Oslo, Norway

^eVienna University of Technology, Vienna, Austria

^fUniversity of Glasgow, Glasgow, U.K.

^gJožef Stefan Institute, Ljubljana, Slovenia

ⁱUniversity of Birmingham, Birmingham, U.K.

^jUniversity of Zagreb, Zagreb, Croatia

^kRheinische Friedrich-Wilhelms Universität Bonn, Bonn, Germany

^lBolu Abant Izzet Baysal University, Bolu, Turkey

^mAix Marseille University, CNRS/IN2P3, CPPM, Marseille, France

ⁿCEA-IRFU, Paris, France

^oDeutsches Elektron-Synchrotron DESY, Hamburg, Germany

E-mail: heinz.pernegger@cern.ch

¹Corresponding author.

ABSTRACT: Depleted Monolithic Active Pixel Sensor (DMAPS) prototypes developed in the TowerJazz 180 nm CMOS imaging process have been designed in the context of the ATLAS upgrade Phase-II at the HL-LHC. The pixel sensors are characterized by a small collection electrode ($3 \mu\text{m}$) to minimize capacitance, a small pixel size ($36.4 \times 36.4 \mu\text{m}^2$), and are produced on high resistivity epitaxial p-type silicon. The design targets a radiation hardness of $1 \times 10^{15} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$, compatible with the outermost layer of the ATLAS ITK Pixel detector. This paper presents the results from characterization in particle beam tests of the Mini-MALTA prototype that implements a mask change or an additional implant to address the inefficiencies on the pixel edges. Results show full efficiency after a dose of $1 \times 10^{15} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$.

KEYWORDS: Front-end electronics for detector readout; Particle tracking detectors (Solid-state detectors); Radiation-hard detectors; Solid state detectors

Contents

1	Introduction	1
2	Sensors with small collection electrodes	2
2.1	Charge collection implant structures in Mini-MALTA	3
2.2	The Mini-MALTA sensor design	3
3	Laboratory measurements	5
3.1	Signal response using ^{55}Fe source	5
3.2	Threshold measurement and tuning	6
3.3	Noise occupancy	8
4	Test beam setup and data analysis	8
4.1	Beam telescope arrangement	8
4.2	Track reconstruction and alignment	10
4.3	Hit to track matching and efficiency calculation	10
5	Efficiency measurements before and after irradiation	11
5.1	Efficiency dependency on implant configuration and pre-amplifier gain	11
5.2	Efficiency dependence on substrate voltage	12
5.3	Efficiency for different threshold settings	13
6	Conclusions	16

1 Introduction

Depleted Monolithic Active Pixel Sensor (DMAPS) prototypes have been developed in the Tower-Jazz 180 nm CMOS imaging process with the aim to explore their viability for the Phase-II upgrade of ATLAS for the High Luminosity LHC [1], and for future HEP experiments [2–4]. With previous developments focusing on low-radiation environments [5], special interest lies now on the radiation hardness of this technology up to 100 Mrad in Total Ionizing Dose (TID) and $\geq 1 \times 10^{15}$ 1 MeV $n_{\text{eq}}/\text{cm}^2$ in Non-Ionizing Energy Loss (NIEL) in order to be used in the harsh environment of these experiments. Monolithic CMOS sensors additionally allow to minimize scattering material for best tracking performance. The developments reported here investigate pixel sensors, dubbed MALTA sensor and Mini-MALTA sensor, with small electrodes (electrode diameter $3 \mu\text{m}$ at $36.4 \mu\text{m}$ pixel pitch).

The advantage of small collection electrodes lies in the resulting small capacitance, which in turn helps to minimize noise and achieve low power dissipation in the active area. However, detection efficiency after irradiation in sensors with small electrodes can be critically affected in the

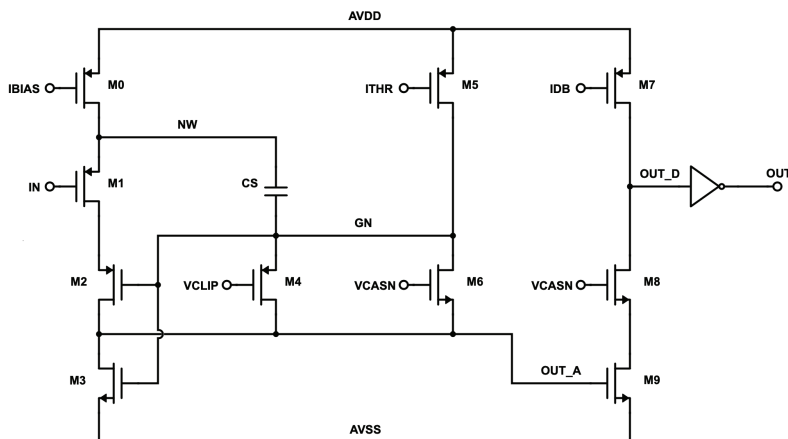


Figure 1. Analog front-end circuit of the MALTA and Mini-MALTA sensors.

pixel corners [6, 7]. To improve this, we designed special p-type and n-type implant geometries [8]. These special implant geometries are implemented in sub-matrices of the Mini-MALTA sensor. The detection efficiency for different pixel designs before and after neutron irradiation are studied in beam tests to determine the optimal pixel design for radiation hard depleted monolithic CMOS sensors.

2 Sensors with small collection electrodes

The small collection electrode minimizes input capacitance to achieve a high Q/C ratio at the circuit input. In the case of a $25\ \mu\text{m}$ thick sensitive layer we expect a most probable ionization charge of around $1500\ e^-$. To calculate the expected ionisation charge for our sensor, we assume an ionisation charge of 63 electron-hole pairs per μm path length [9]. With a total electrode capacitance of 5 fF this results in a voltage step of around 50 mV. This offers the possibility of using an open-loop voltage amplifier as the first amplification stage, instead of the conventional charge-sensitive amplifier scheme with a feedback capacitor, to save space and simplify the circuit. The collection electrode input voltage is reset after a particle hit using a diode-circuit or a PMOS-transistor. The front-end (FE) amplifier output connects to a discriminator, which produces the digital signal for a hit pixel. The discriminator threshold is set globally for the full sensor. The analog FE circuit is shown in figure 1.

Initial measurements of this circuit on the MALTA sensor revealed significant Random-Telegraph-Signal (RTS) noise preventing lower threshold settings. This was attributed to the “M3” transistor being much smaller than on previous circuits. To verify this assumption the Mini-MALTA sensor includes sectors with the same “M3” size as on MALTA and larger. Measurements on the Mini-MALTA sensor confirmed that the larger transistor sizes significantly decreased the RTS noise, both before and after irradiation. In addition, the larger NMOS size also yielded a significantly larger gain and lower charge threshold for the same settings. Further measurements confirmed the “M3” output conductance was higher than expected, which caused gain degradation for the FE. In addition it was found that for lower threshold settings, where the influence of this output conductance is larger, the spread on the gain and hence the threshold spread increased.

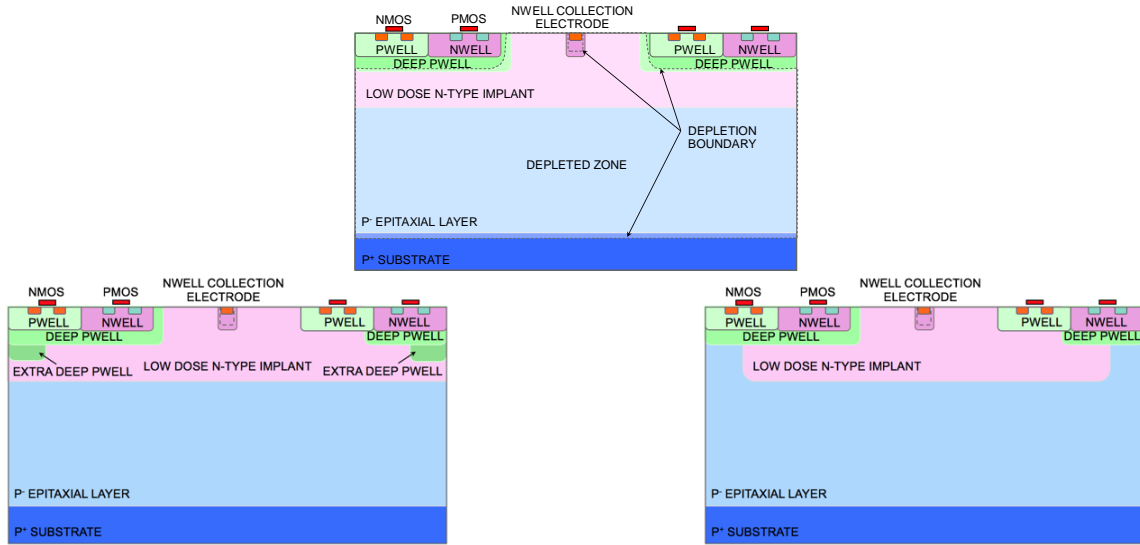


Figure 2. Cross section of the TowerJazz process: continuous n- layer (top), with extra deep p-well at the edge of the pixel (bottom left) and with the low dose n-implant removed (n^- gap) at the edge of the pixel (bottom right).

2.1 Charge collection implant structures in Mini-MALTA

Figure 2 (top) shows the cross-section of the TowerJazz process with a special low-dose n -type implant addition across the full pixel matrix [3]. This implant generates the junction to deplete the epitaxial silicon layer ($25\ \mu\text{m}$ thickness). This n^- layer separates the deep p-well of the pixel circuit from the p-type substrate. The substrate is reverse biased (0 to $-20\ \text{V}$) to fully deplete the epitaxial layer of the entire pixel. We refer to this implant configuration as “standard continuous n- layer”. The deep p-well is biased in our measurements at $-2\ \text{V}$. The n^- layer is depleted from its junction to deep-p-well and p-type epitaxial layer. Depending on the choice of n^- layer doping concentration the n^- layer may not be fully depleted near the electrode at $-2\ \text{V}$, which influences capacitance and gain. Changing the p-well voltage to $-6\ \text{V}$ in future prototypes is expected to improve charge collection and reduce capacitance.

The TowerJazz process can be further modified (as shown in figure 2 bottom row) by adding a gap in the low dose n-layer through a mask change (lower right) or adding an additional production process compatible deep p-type implant (lower left). We refer to these configurations as “ n^- gap” and “extra deep p-well” configurations, respectively. The purpose of these modifications is to improve the charge collection at the pixel edges and corners through the creation of a stronger lateral field, which focuses the ionization charge towards the collection electrode. The design of these implant structures has been optimized in TCAD simulations [8], which indicate that these modifications significantly improve the charge collection at the pixel boundaries.

2.2 The Mini-MALTA sensor design

The Mini-MALTA chip matrix contains 16×64 square pixels with a pitch size of $36.4\ \mu\text{m}$. The full chip measures $1.7 \times 5\ \text{mm}^2$ including periphery blocks for data handling, sensor configuration and biasing.

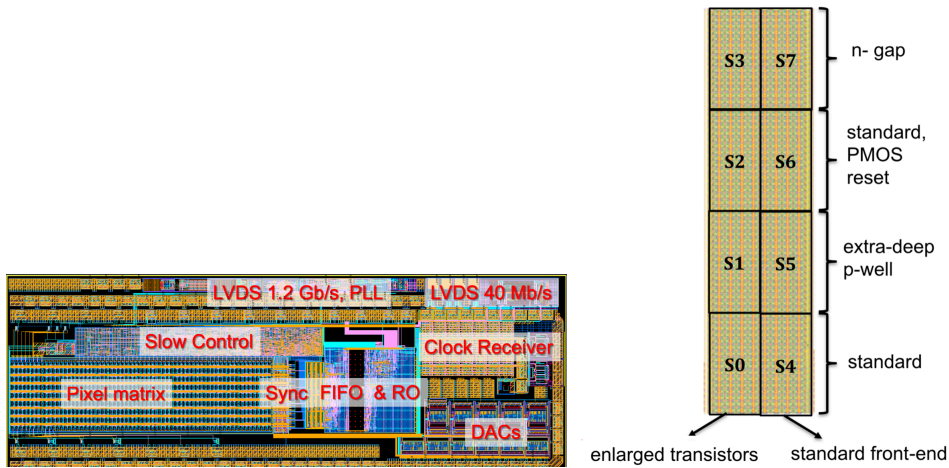


Figure 3. Top view of the full Mini-MALTA chip (left). Layout of the Mini-MALTA pixel matrix at the read-out level and pixel sub-groups of 8×16 pixels (right).

The Mini-MALTA sensor comprises eight different pixel flavours differing in analog FE design, reset mechanism and electrode/well geometries, as detailed in table 1. They are implemented in the matrix as 8×16 pixel groups as illustrated in figure 3.

Table 1. Pixel sub-groups in the Mini-MALTA pixel matrix.

Sector ID	Pre-amp design	Reset type	Implant configuration
0	enlarged transistor FE	diode reset	continuous n^- layer
1	enlarged transistor FE	diode reset	extra deep p-well
2	enlarged transistor FE	PMOS reset	continuous n^- layer
3	enlarged transistor FE	diode reset	n^- gap
4	standard transistor FE	diode reset	continuous n^- layer
5	standard transistor FE	diode reset	extra deep p-well
6	standard transistor FE	PMOS reset	continuous n^- layer
7	standard transistor FE	diode reset	n^- gap

Each pixel contains a charge collection electrode formed by an n-well of 3 micron diameter, contacted by an n^+ region to the readout circuit. The n-well itself forms the contact to the lightly doped n-implant below. Reverse bias depletes the lightly doped n- region and also some part of the n-well. The undepleted remainder of the n-well then collects the signal charge.

The collection electrode is connected to the analog FE circuit, which is located in a separate deep p-well. The output of the analog circuit connects to the digital circuit, which buffers the discriminator output of the FE-circuit and transmits a digital signal to the end-of-column logic. The pixels are organized in groups of 2×8 . Hits from pixels are sent to dedicated logic, common within the group, generating a reference pulse (1 bit) as well as a pixel address (16 bit where each bit corresponding to a particular pixel out of the 16 pixels in each group) and group address (5

bit) signal on the 22-bit wide double-column bus. Digital signals on this bus are 2ns wide and are transmitted asynchronously to the periphery [6]. No clock is distributed over the matrix to minimize power consumption and avoid cross-talk between digital and analog circuit. The digital signal from the pixel is stored in the end-of-column logic memory: the data from the groups are stored asynchronously into 16 synchronization memories, which are then read out synchronously with the external 320 MHz clock using a priority encoder. Inside the synchronization memory, the precise time-of-arrival information is added by latching the value of a 4-bit counter running at 640 MHz. When reading out the hits, the priority encoder gives priority to leftmost pixel groups (see figure 3 right) in case of simultaneous hits in multiple memories. In the end-of-column logic the 4-bit double-column address is added to the data words, along with 3 bit bunch-crossing counter information (BCID) which is generated in the synchronization memories by using the external 40 MHz clock. The data from the end-of-column logic is stored into a FIFO with a depth of 64 48-bit words.

By default, the Mini-MALTA operates in ‘fast’ readout mode where the 48-bit 8b/10b encoded data is sent off from the chip at 1.2 Gbps. In this case a 600 MHz clock, which is generated from the external 40 MHz clock, is used to send the data at double data rate. The Mini-MALTA sensor also offers the possibility to output the data at 40 Mbps for setups where fast signal transmission is not necessary nor desirable. This mode was used for beam tests reported here. To mark the beginning and end of the sent 48-bit words, a dedicated ‘acknowledge’ output signal is used, which is active only during the 48×25 ns when the data is being transmitted.

3 Laboratory measurements

3.1 Signal response using ^{55}Fe source

The response of the sensors is verified using photons from a ^{55}Fe source and dedicated “test-pixels” with analog readout. ^{55}Fe produces photons with two characteristic lines, K_α and K_β , having energies of 5.9 keV and 6.5 keV respectively. The K_α peak is the dominant decay mode. The Mini-MALTA test-pixels allow to probe the analog signal before the discriminator (“OUT-A” in figure 1) and at the collection electrode (“IN” in figure 1).

Figure 4 (left) shows the signal amplitude spectrum from the test pixels measured on “OUT-A” with enlarged NMOS transistors for unirradiated Mini-MALTA samples in comparison to preamplifiers with standard (minimal-size) transistors. As explained earlier, enlarging the NMOS transistor “M3” significantly improves gain and gain uniformity and also RTS noise and therefore allows operation at lower thresholds. Clear peaks from K_α and K_β lines of ^{55}Fe are visible for the unirradiated chip.

Figure 4 (right) shows the signal amplitude spectrum from the test pixels measured on “OUT-A” with enlarged NMOS transistors for unirradiated and neutron irradiated sensors. The sensors received for 1×10^{15} and 2×10^{15} 1 MeV $n_{\text{eq}}/\text{cm}^2$ fluence an additional 1 Mrad and 2 Mrad of TID through the gamma background in the reactor. For the irradiated Mini-MALTA sensors, a clear increase in noise is observed, resulting in an increased width of both peaks. Moreover, there is a shift in the mean peak position visible after irradiation, which suggests that the irradiated Mini-MALTA sensors increase in gain by 20% when operated at the same preamplifier setting. For comparison the amplitude spectrum was also measured at the collection electrode, so at the input of the readout

circuit (“IN”), for unirradiated and irradiated sensors, which also showed a 20% higher ^{55}Fe -signal for the irradiated sensors. Most likely it points to a change in sensor capacitance due to changes in effective doping concentration, rather than a gain change in the readout circuit.

The chip configurations used in figure 4 (left) and in figure 4 (right) were slightly different, resulting in some shift in mean peak position for unirradiated sensors and regions with enlarged NMOS transistors.

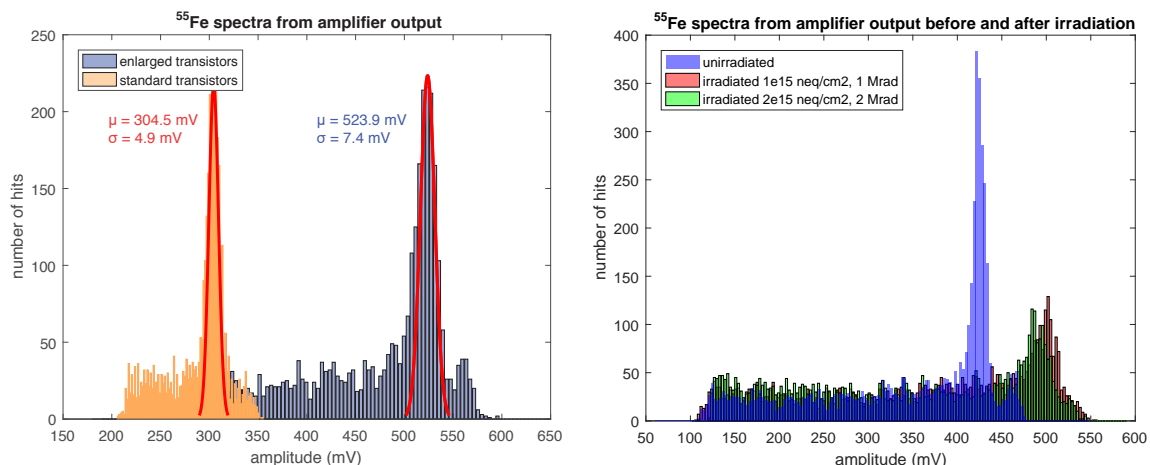


Figure 4. Signal amplitude distribution in response to an ^{55}Fe source as measured on monitoring pixels after the amplifier. The left plot compares the response of the unirradiated sensor for enlarged (sector 0) and standard transistor FE (sector 5). The right plot shows the response for the unirradiated and neutron-irradiated Mini-MALTA samples at sector 0. The chips were operated at -6 V SUB voltage at -20°C temperature and with identical FE settings for each plot.

3.2 Threshold measurement and tuning

The threshold in the full pixel matrix is modified through dedicated on-chip 8-bit DACs which adjust the biasing of the pre-amplifier stage and in-pixel discriminator. The main threshold adjustment is carried out through the discriminator bias current (“IDB”), which is set globally for the full matrix. For the beam test measurements described in the following sections, the chips are tuned to different thresholds to test efficiency as function of applied threshold.

The resulting threshold is measured for each pixel by injecting pulses with varying voltage amplitude on an in-pixel test capacitance (0.23 fF) at the input of each preamplifier. For each pixel, 200 injections per test pulse amplitude are performed, and the threshold point corresponding to 50% occupancy (50% probability of a pixel being fired) is determined by fitting a Gauss error function to the hit occupancy S-curve. The width parameter (to deduce the value of equivalent noise charge ENC) is also extracted from the fit.

Figure 5 shows the measured threshold distributions for unirradiated and neutron irradiated Mini-MALTA samples, separately for sensor regions with standard (right plot) and enlarged transistors (left plot). Default chip tuning configuration is used for all sensors. The sensors were operated at -6 V substrate voltage in a climatic chamber set at -20°C . The gaussian fits are performed to the threshold distributions for each chip. For regions with standard transistors the average threshold

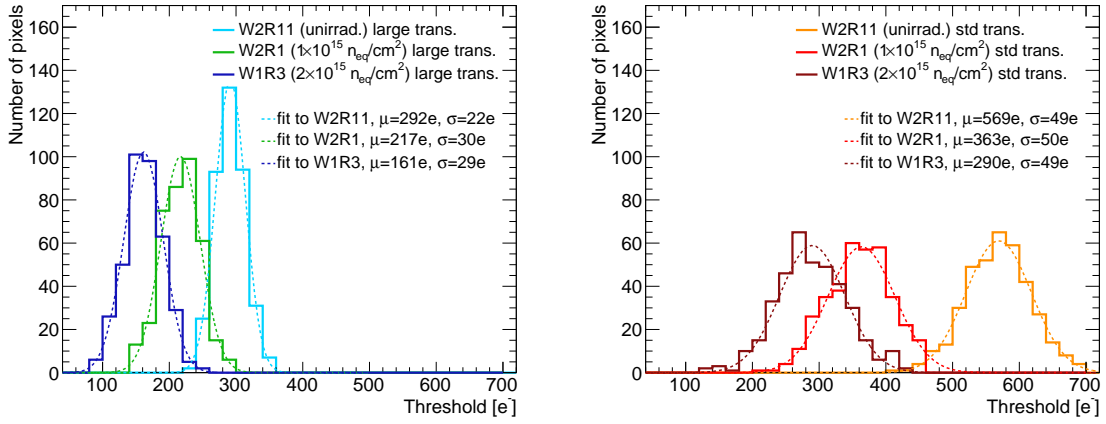


Figure 5. Threshold distributions for unirradiated and neutron-irradiated Mini-MALTA samples at 1×10^{15} and 2×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$. Gaussian fits to threshold distributions are shown as dashed lines. The default chip tuning configuration is used (IDB=100) for unirradiated and irradiated sensors in the plots. Sensor regions with enlarged (left) and standard (right) transistors are shown.

extracted from fit decreases from $570e^-$ (unirradiated) to $360e^-$ (1×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$) and $290e^-$ (2×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$). As already mentioned most of this change is due to a change in the sensor capacitance rather than in the readout circuit. In all regions with enlarged transistors the average threshold values are systematically lower due to the higher gain of the FE circuit with enlarged transistors: $290e^-$ (unirradiated), $220e^-$ (1×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$) and $160e^-$ (2×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$). The threshold dispersion extracted from the gaussian fit is larger for regions with standard transistors (around $50e^-$) than for regions with enlarged transistors ($20\text{-}30e^-$).

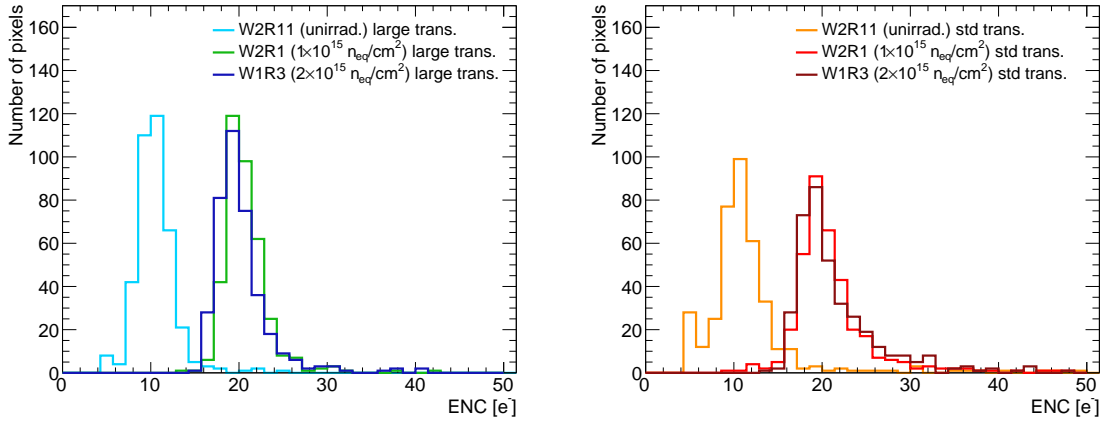


Figure 6. ENC distributions for unirradiated and neutron-irradiated Mini-MALTA samples at 1×10^{15} and 2×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$. Sensor regions with enlarged (left) and standard (right) transistors are shown. The chips were operated at -6 V SUB voltage, -20°C and with same settings.

The ENC distributions for unirradiated and irradiated Mini-MALTA sensors are shown in figure 6. The most probable ENC value before irradiation is $11e^-$ and increases to $\approx 20e^-$ for chips after irradiation. Moreover, the ENC dispersion is lower in the regions with enlarged transistors

($\sigma_{\text{ENC}} \approx 3e^-$). The ENC distributions in sectors with standard transistors ($\sigma_{\text{ENC}} \approx 5e^-$) show a significant tail of pixels with high noise. We attribute this to Random Telegraph Signal noise (RTS) due to the use of minimal-size transistors in parts of the analog circuit. The measurements on sectors with enlarged transistors show that increasing the size of these transistors significantly reduces RTS noise and ENC dispersion as illustrated in figure 6 (left).

3.3 Noise occupancy

The noise level for each Mini-MALTA chip is characterized by measuring the number of noisy pixels as a function of charge threshold. The noisy pixels with relatively large noise rate (above 0.5 kHz) are masked and are not counted in the following. For each chip these masked pixels constitute less than 1% of the total number of pixels. Figure 7 presents the distribution of the number of noisy pixels as a function of charge threshold for various Mini-MALTA samples, separately for sensor regions with enlarged and standard transistors. Typically for unirradiated Mini-MALTA chips, no more than 1 or 2 noisy pixels are observed even at very low thresholds ($\approx 100e^-$). For the neutron-irradiated Mini-MALTA sensors, the number of noisy pixels is low at higher thresholds (less or equal one), and the number grows with decreasing the threshold. At lowest thresholds there are 3–5 noisy pixels (out of 384 measured pixels) for each region of the neutron-irradiated Mini-MALTA sensors.

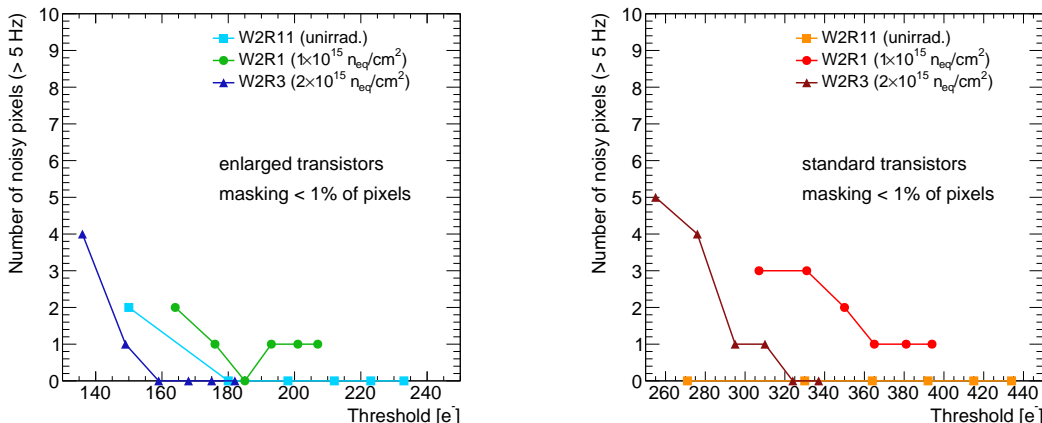


Figure 7. Distribution of the number of noisy pixels (with rate above 5 Hz) for unirradiated and neutron-irradiated Mini-MALTA samples at 1×10^{15} and 2×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$. Sensor regions with enlarged (left) and standard (right) transistors are shown. For all chips, less than 1% of total pixels in a given region are masked due to noise above 0.5 kHz, and these pixels are not counted in the procedure. The chips were operated at -6 V SUB voltage and -20°C .

4 Test beam setup and data analysis

4.1 Beam telescope arrangement

The data presented in this study were recorded at the ELSA test beam facility at the University of Bonn. The ELSA synchrotron circulates one electron bunch with a maximum energy of about 3.5 GeV. The test beam is generated via a twofold conversion and the detectors were probed with

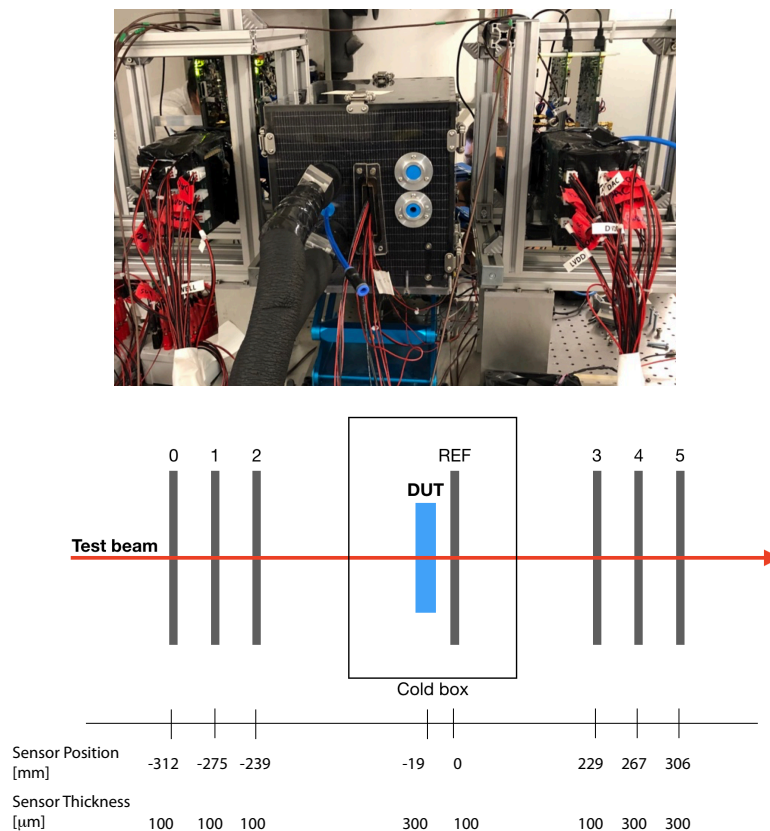


Figure 8. Photo of the test beam setup (top) and its graphical diagram (bottom) showing the beam telescope with seven MALTA tracking planes and the device under test (DUT) between the upstream (3 planes), reference (1 plane, REF) and downstream (3 planes) arms of the telescope. The DUT and the reference MALTA plane are placed in the cold box, operated at -20°C .

2 GeV electrons. The test beam setup is shown in figure 8. The beam telescope based on six MALTA planes was used. Electrons first passed through 3 MALTA silicon detector planes, before entering the Device Under Test (DUT) and one extra MALTA reference plane (REF) placed close in front of the DUT. A REF plane close to the DUT improves the position resolution of the telescope when using the low-energy electron beam. The DUT and REF planes are placed in the cold box which was operated at -20°C . Another 3 MALTA planes are placed downstream of the DUT and are used together with the upstream planes as reference system for track reconstruction. To minimize multiple scattering $100\ \mu\text{m}$ thin sensors were used when possible. Figure 8 also gives the sensor position along the beam axis as well as the sensor thickness for each plane.

Each MALTA sensor provides a fast trigger signal when there is a hit on the plane. Upon coincidence of 2 or 3 planes, a trigger signal initiates the readout of the entire system. The data acquisition is performed using a custom read-out system based on the Xilinx VC707 boards and fast software [10–12].

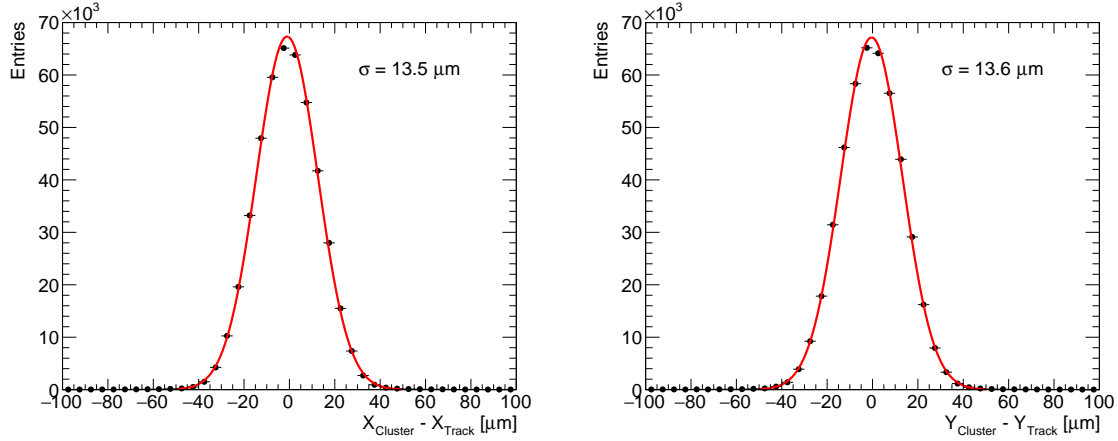


Figure 9. Difference between the expected X- (left) and Y- (right) position of the track in the Mini-MALTA plane and the position of the closest cluster center. The gaussian fit (red lines) yields $\sigma_X = 13.5 \mu\text{m}$ and $\sigma_Y = 13.6 \mu\text{m}$.

4.2 Track reconstruction and alignment

Tracks are selected by requiring a hit on the third plane of the telescope in front of the DUT (plane ‘2’ from figure 8), and hits in the first two planes after the DUT (plane ‘REF’ and plane ‘3’ from figure 8). Adjacent pixel hits are combined into clusters. The track reconstructed from these three telescope layers is extrapolated to the plane of the DUT, taking into account multiple scattering by using the General Broken Lines (GBL) formalism [13, 14]. The track trajectory calculation uses the material description of the DUT and all telescope planes as well as the electron beam energy for multiple scattering estimation.

The alignment of telescope planes uses a two-step method. In the first step, a coarse alignment is performed, where the hits in X and Y of all neighboring telescope plane combinations are correlated and the resulting residual distributions are shifted with their means towards zero. The second step uses full telescope tracks and a χ^2 minimization method for fine alignment. This returns the alignment parameters and uncertainties for each of the telescope planes. The residual distribution between the telescope track projection and the center of the nearest cluster, which is not used in the track reconstruction, has a width of $\approx 13.5 \mu\text{m}$ in both X and Y directions, as shown in figure 9. The width of the residual distributions is dominated by the expected intrinsic DUT resolution of $10.5 \mu\text{m}$.

4.3 Hit to track matching and efficiency calculation

The hit detection efficiency is defined as the fraction of clusters on the DUT matched to telescope tracks over the total number of tracks. Reconstructed tracks with $\chi^2/dof < 10$ are used in the efficiency calculation. A cluster in DUT is matched to a track if the distance between the position of a track interpolated to the plane of the DUT and the position of the center of the cluster is smaller than $100 \mu\text{m}$.

The acceptance area of the DUT is folded into the efficiency calculation as follows: due to the finite track resolution of the beam telescope, all tracks with a hit prediction on a DUT edge pixel are removed from the analysis. An additional exclusion area of the size of two pixel rows

is also applied between the neighboring DUT sensor sectors of different designs. Tracks with hit predictions on noisy pixels (radius of $36.4 \mu\text{m}$ around the noisy pixel center) are rejected from the efficiency analysis. Given the limited size of our sensor acceptance in each sector (14×6 pixel after removal of edge pixels) a single noisy pixel can influence the efficiency calculation.

5 Efficiency measurements before and after irradiation

5.1 Efficiency dependency on implant configuration and pre-amplifier gain

Figure 10 (left) shows the efficiency as a function of the track position in the DUT plane for an unirradiated Mini-MALTA sensor (“W2R11”) tuned to an example threshold of $200e^-$ on sectors with enlarged transistors and $380e^-$ on sectors with standard, i.e. minimum size, transistors. The measured sector efficiency for an unirradiated chip and standard transistors were $97.9 \pm 0.1\%$ for the continuous n-layer, $98.9 \pm 0.1\%$ for the extra deep p-well and $99.1 \pm 0.1\%$ for the n^- gap.

For sensor regions with enlarged transistors the average efficiency is $99.6 \pm 0.1\%$ at a threshold of $200e^-$ and does not depend on extra sensor modification. The small inefficiency is partly due to relatively tight cluster-to-track matching conditions which accounts for 0.2% efficiency loss, and partly due to small regional inefficiency at double-column boundaries ($\approx 0.2\%$ overall efficiency reduction) which is still under investigation.

The 2D efficiency map for a $1 \times 10^{15} \text{ 1 MeV } n_{\text{eq}}/\text{cm}^2$ neutron irradiated Mini-MALTA sensor (“W2R1”) is shown in figure 10 (right).

Table 2 lists the measured efficiency at given threshold values for all Mini-MALTA sensors used in the beam tests in dependency of the implant configuration and FE amplifier design.

Table 2. Summary of the efficiency measurements for various Mini-MALTA chips. The values are shown separately for different sensor regions. All chips were operated at low threshold settings. The uncertainties listed are statistical.

Chip ID	EPI [μm]	Fluence [$1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$]	SUB [V]	Process modification	Efficiency (enlarged trans. region) [%] / threshold [e^-]	Efficiency (standard trans. region) [%] / threshold [e^-]
W2R11	30	unirrad.	-6	n^- gap	$99.6 \pm 0.1 / 200e^-$	$99.1 \pm 0.1 / 380e^-$
				extra deep p-well	$99.6 \pm 0.1 / 200e^-$	$98.9 \pm 0.1 / 380e^-$
				continuous n^-	$99.6 \pm 0.1 / 200e^-$	$97.9 \pm 0.1 / 380e^-$
W2R1	30	1×10^{15}	-6	n^- gap	$97.6 \pm 0.1 / 105e^-$	$86.5 \pm 0.1 / 210e^-$
				extra deep p-well	$97.9 \pm 0.1 / 105e^-$	$87.0 \pm 0.1 / 210e^-$
				continuous n^-	$91.9 \pm 0.1 / 105e^-$	$78.8 \pm 0.2 / 210e^-$
W4R2	25	1×10^{15}	-6	n^- gap	$98.8 \pm 0.1 / 120e^-$	$90.7 \pm 0.1 / 275e^-$
				extra deep p-well	$99.2 \pm 0.1 / 120e^-$	$92.5 \pm 0.1 / 275e^-$
				continuous n^-	$95.8 \pm 0.1 / 120e^-$	$79.4 \pm 0.2 / 275e^-$
W5R3	25	2×10^{15}	-10	n^- gap	$92.1 \pm 0.2 / 120e^-$	$73.1 \pm 0.3 / 230e^-$
				extra deep p-well	$93.7 \pm 0.2 / 120e^-$	$76.4 \pm 0.3 / 230e^-$
				continuous n^-	$86.5 \pm 0.2 / 120e^-$	$70.9 \pm 0.3 / 230e^-$

After 1×10^{15} 1 MeV n_{eq}/cm^2 neutron irradiation, the average efficiency significantly decreases for regions with standard transistors due to the lower gain (higher effective threshold) in these sectors: it reaches 78.8% in the region with no extra sensor modification, 87.0% with extra deep p-well and 86.5% with n^- gap. While the modifications to the implant proof effective, the overall efficiency is still significantly affected by the high threshold. As expected, the inefficiency is mainly present in regions around the pixel edges and corners, as shown in figure 11 where the in-pixel efficiency plots are shown. The 2×2 pixel plots overlap with the double column structure of the chip matrix. Along the pixel edge and in particular in the corners the charge is shared between two or more pixels. The resulting small per-pixel signals are suppressed by a high effective threshold leading to inefficiency. For regions with enlarged transistors the average efficiency is 91.9% in the region with no extra sensor modification, 97.9% with extra deep p-well and 97.6% with extra n^- gap. It is therefore clear that the usage of enlarged transistors significantly increases efficiency for sensors after irradiation due to the higher gain, lower gain spread and reduced RTS noise. In the implant configuration with a continuous n^- layer and no extra deep p-well (sector 0) the overall efficiency is still reduced in the corner. If the charge collection in the pixel corners is improved through either a gap in the n^- layer or an extra deep p-well along the pixel borders (see figure 2 bottom row), the sensor becomes nearly full efficient at 1×10^{15} 1 MeV n_{eq}/cm^2 . Figure 10 also shows the number of noisy pixels through white bins in the different sectors, where the track prediction is rejected and no efficiency is calculated. We observe on the irradiated sensor (“W2R1”) noisy pixels only in the area of standard FE. In the area with enlarged transistors, no noisy pixels are visible. This provides another indication that enlarging some crucial NMOS transistors helps to reduce RTS noise. After 2×10^{15} 1 MeV n_{eq}/cm^2 neutron irradiation, shown for sensor “W5R3” at different thresholds in figure 12, we observe an efficiency reduction to $\approx 93\%$ also in the sector with extra deep p-well and $\approx 92\%$ in the sector with n^- gap. All other sectors are affected by this efficiency reduction as well. The higher charge thresholds further degrade the efficiencies in the sectors with the lower gain pre-amplifier, especially after irradiation.

5.2 Efficiency dependence on substrate voltage

The efficiency is also studied as function of the substrate voltage. From TCAD simulations we expect best charge collection at a substrate voltage of around -10 V [8]. Higher substrate voltage leads to a strong vertical electric field but reduces the relative lateral field. The result of a higher substrate voltage is a much more vertical field that pushes charge generated near the pixel corners/edges into the low field region under the p-well at those locations. The charge takes time to escape from these regions and this decreases efficiency especially after irradiation as then charge is more easily captured by radiation induced traps.

In figure 13 we show the results for neutron irradiated Mini-MALTA samples at 1×10^{15} and 2×10^{15} 1 MeV n_{eq}/cm^2 . For the chip irradiated at 1×10^{15} 1 MeV n_{eq}/cm^2 the efficiency is relatively stable when changing the substrate voltage between -6 V and -10 V. In contrast, the chip irradiated at 2×10^{15} 1 MeV n_{eq}/cm^2 has best efficiency around -10 V to -12 V. The efficiency decreases at higher (-6 V) and lower (-20 V) SUB voltages in most of the sectors which confirms the qualitative observations in TCAD simulations. Therefore, the non-irradiated and irradiated Mini-MALTA samples at 1×10^{15} 1 MeV n_{eq}/cm^2 were operated at a substrate voltage of -6 V, whereas the samples irradiated at 2×10^{15} 1 MeV n_{eq}/cm^2 had a substrate voltage of -10 V applied.

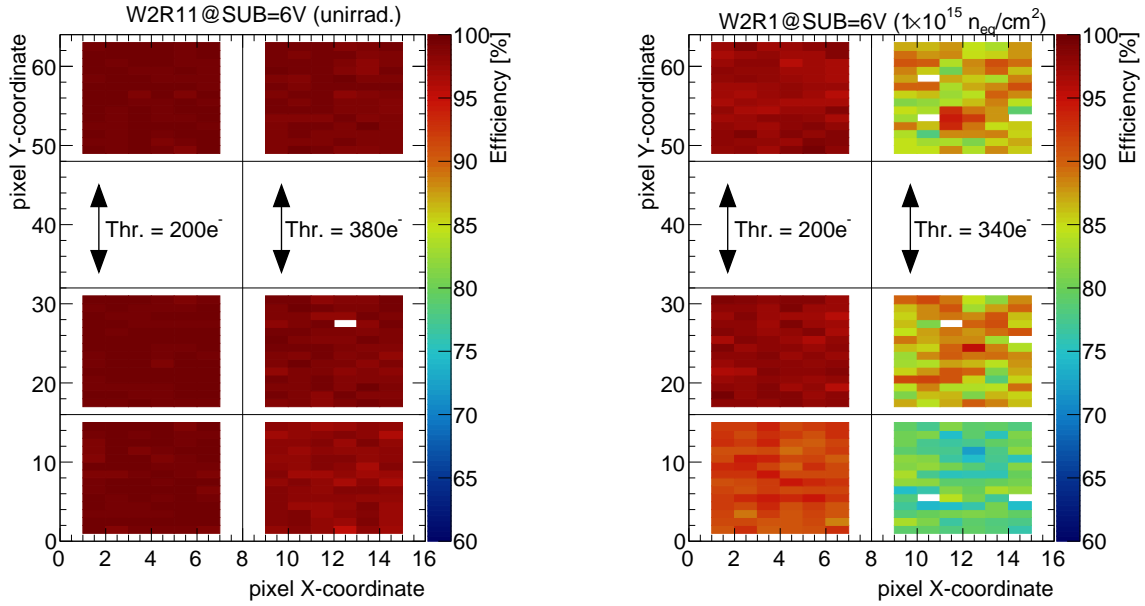


Figure 10. 2D efficiency maps for non-irradiated (left) and irradiated Mini-MALTA samples at 1×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$ (right). Different sensor regions are visible: standard MALTA-like (bottom part of each chip), modified with extra deep p-well (middle part) and modified with extra n^- gap (top part). Results are also shown for sensor regions with standard (right side of each chip) and enlarged (left side) transistors. The chips were operated at -6 V substrate voltage and -20°C , and were tuned for low threshold.

5.3 Efficiency for different threshold settings

The efficiency is significantly affected by the preamplifier design, and here in particular the size of the NMOS transistor “M3” influencing gain, gain uniformity and RTS noise, ultimately allowing lower threshold operation to achieve higher efficiency. Furthermore, the additional deep p-type implant or n^- gap at the pixel edges improves the charge collection and efficiency after irradiation. The efficiency as a function of threshold for 1×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$ irradiated Mini-MALTA samples is shown in figure 14. With lowering the threshold, the efficiency increases and can reach approximately 95% for continuous n^- sectors with enlarged transistors and 98–99% for sectors with n^- gap or extra deep p-well. The gain is due to better charge collection in the pixel corners caused by the modifications of implants on the pixel edge.

When using minimal size transistors we reach only 88–92% efficiency for n^- gap or extra deep p-well pixel designs even at thresholds around $200 e^-$ whereas the preamplifier design with enlarged transistors reaches 98%. This highlights the importance of transistor choice in our pre-amplifier circuit, most notably the “M3” transistor which needs to be chosen for lowest output conductance. The sector with continuous n^- and standard transistor behaves worst, due to the inefficient charge collection in the pixel corners and high threshold.

Similar trends are visible for neutron irradiated Mini-MALTA samples at 2×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$ (figure 15). In this case the best efficiency is obtained for modified regions with extra deep p-well and amounts up to 75% for regions with standard-size transistors and up to 94% for regions with enlarged transistors.

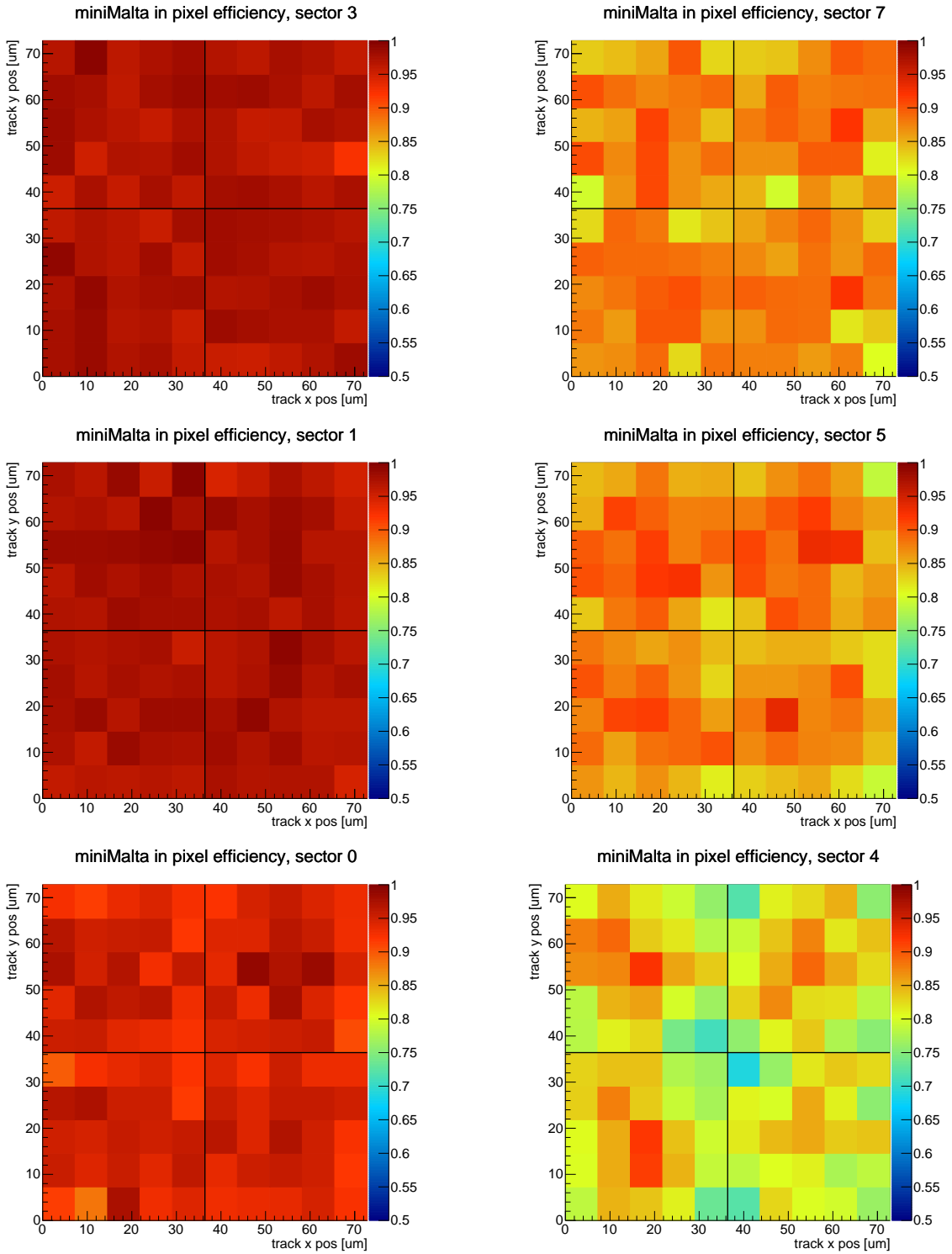


Figure 11. In-pixel 2D efficiency maps for irradiated Mini-MALTA sample at 1×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$ for 2×2 pixel groups. Different sensor regions are shown: standard MALTA-like (bottom part of each chip), modified with extra deep p-well (middle part) and modified with extra n^- gap (top part). Results are also shown for sensor regions with standard (right side of each chip) and enlarged (left side) transistors. The binning corresponds to 5×5 entries per single pixel. The chip was operated at -6 V substrate voltage and -20°C .

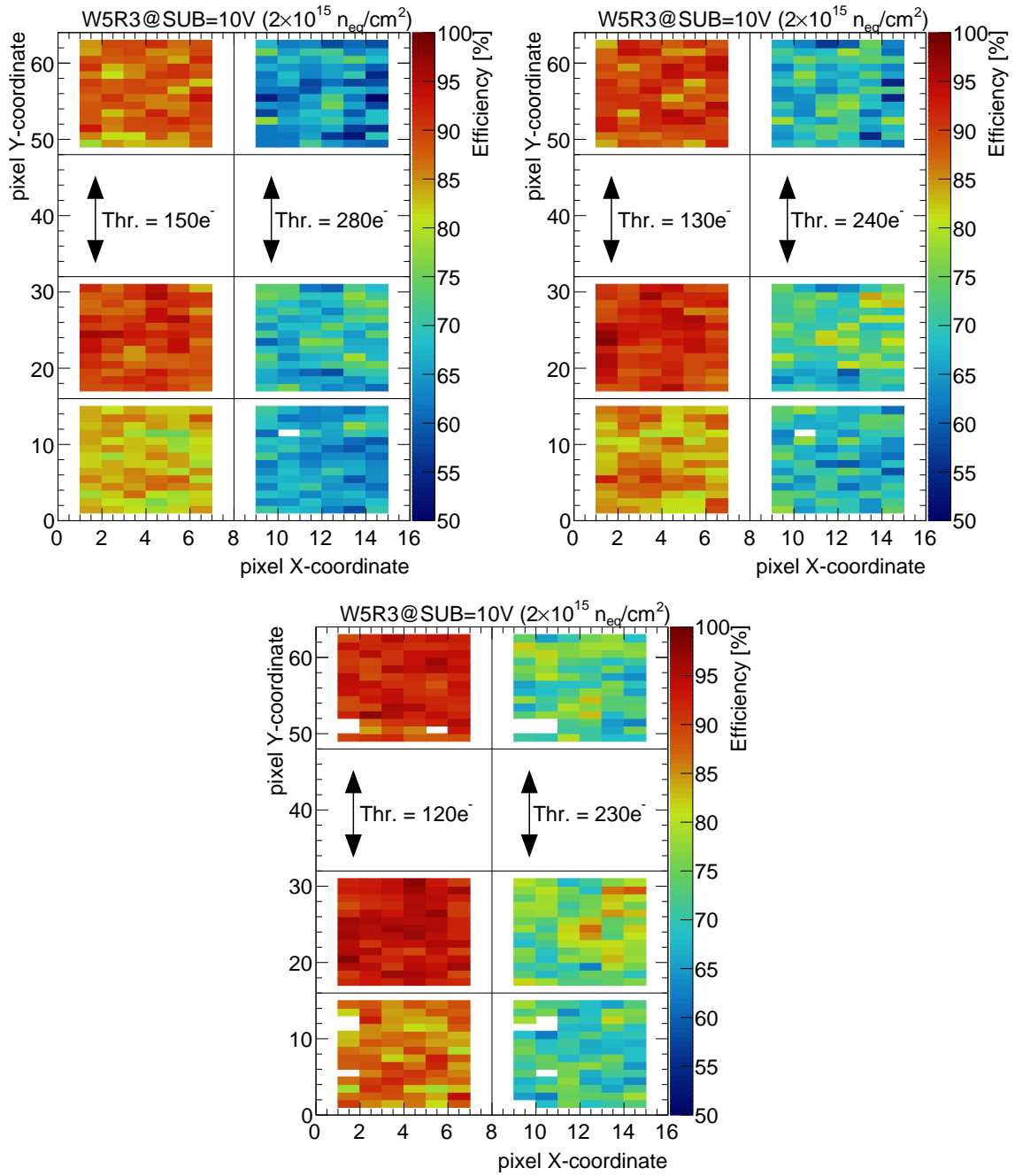


Figure 12. 2D efficiency maps for irradiated Mini-MALTA sample at 2×10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$ at various threshold settings. Different sensor regions are visible: standard MALTA-like (bottom part of each chip), modified with extra deep p-well (middle part) and modified with extra n^- gap (top part). Results are also shown for sensor regions with standard (right side of each chip) and enlarged (left side) transistors. The binning corresponds to one entry per single pixel. The chip was operated at -10 V substrate voltage and -20°C .

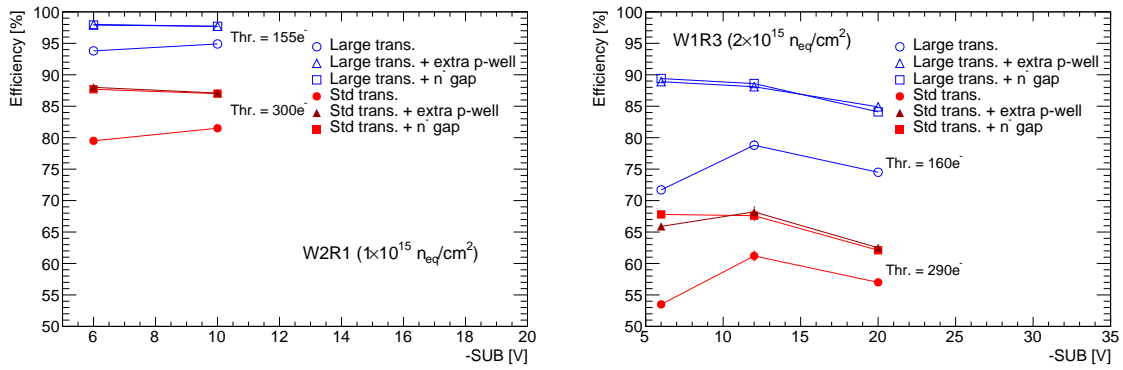


Figure 13. Efficiency versus SUB voltage for neutron irradiated Mini-MALTA samples at 1×10^{15} 1 MeV n_{eq}/cm^2 (left) and 2×10^{15} 1 MeV n_{eq}/cm^2 (right). Different sensor regions are presented: standard MALTA-like (circles), modified with extra deep p -well (triangles) and modified with extra n^- gap (rectangles). Results are also shown for sensor regions with standard (open markers) and enlarged (full markers) transistors.

In these measurements we also observe that sensors with $25 \mu m$ epitaxial layer produce similar or slightly better efficiency than sensors produced on $30 \mu m$ epitaxial wafers at the same substrate voltage, despite the fact that we expect about 20% more ionization charge in the $30 \mu m$ epitaxial wafers. This effect may be due to the higher field in the thinner epitaxial layer. Additionally the choice of processing for the creation of the low-doped n^- layer may contribute to the observed behaviour: for sensors produced on $25 \mu m$ epitaxial wafers we have chosen a slightly deeper n^- implantation than in the $30 \mu m$ epitaxial wafers. A deeper n^- layer moves the junction deeper in the high resistivity epitaxial layer which provides a better field configuration for charge collection in the pixel corners.

6 Conclusions

This paper presents measurement results on the Mini-MALTA Monolithic Active Pixel Sensor prototype developed in the TowerJazz 180nm CMOS imaging process. The prototype implements several improvements to address the inefficiencies and limitations of the previous prototypes. In particular charge collection is improved in the pixel corners by modifying implants along the pixel boundary (n^- gap or extra deep p -well pixel designs), and the charge sensitive FE is improved by increasing the size of an NMOS transistor yielding lower RTS noise, higher gain and lower threshold spread allowing operation at lower thresholds.

The measurement results demonstrate that with these improvements the sensors achieve a 98-99 % efficiency at a threshold of $100e^-$ to $150e^-$ after a dose of 1×10^{15} 1 MeV n_{eq}/cm^2 . To achieve full efficiency at 2×10^{15} 1 MeV n_{eq}/cm^2 the FE should be further improved to achieve thresholds below $100e^-$.

Acknowledgments

The authors are grateful to the University of Bonn for the support received during measurements performed at the E3 beam-line at the electron accelerator ELSA operated by the university of Bonn

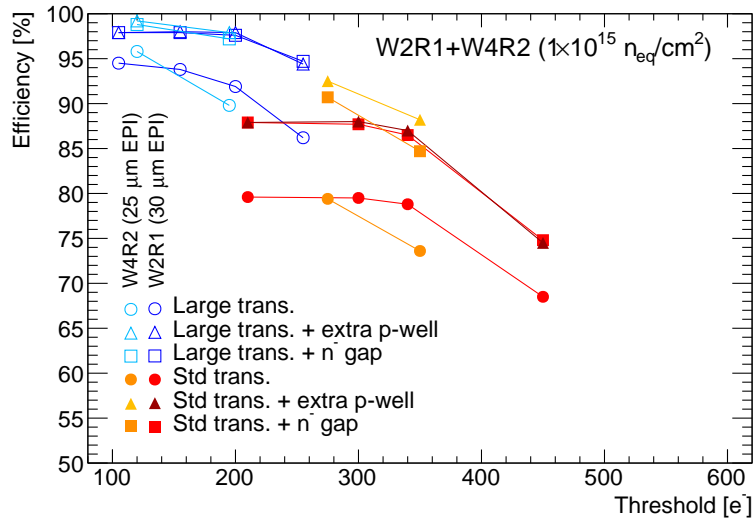


Figure 14. Efficiency versus threshold mean for neutron irradiated Mini-MALTA samples at 1×10^{15} 1 MeV $n_{\text{eq}}/\text{cm}^2$ (-6 V substrate voltage, -20°C). Different sensor regions are presented: standard MALTA-like (circles), modified with extra deep p-well (triangles) and modified with extra n^- gap (rectangles). Results are also shown for sensor regions with standard (open markers) and enlarged (full markers) transistors, as well as for sensors with different epitaxial layer thicknesses: $25 \mu\text{m}$ (orange or light blue symbols) and $30 \mu\text{m}$ (red or dark blue symbols).

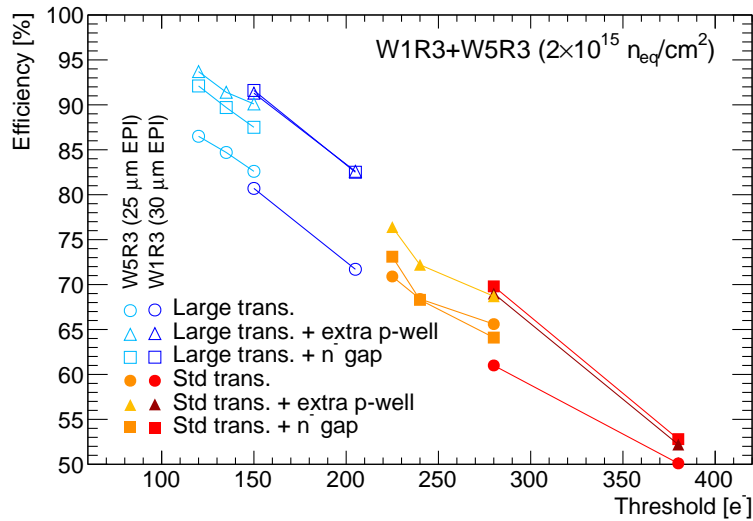


Figure 15. Efficiency versus threshold mean for neutron irradiated Mini-MALTA samples at 2×10^{15} 1 MeV $n_{\text{eq}}/\text{cm}^2$ (-10 V substrate voltage, -20°C). Different sensor regions are presented: standard MALTA-like (circles), modified with extra deep p-well (triangles) and modified with extra n^- gap (rectangles). Results are also shown for sensor regions with standard (open markers) and enlarged (full markers) transistors, as well as for sensors with different epitaxial layer thicknesses: $25 \mu\text{m}$ (orange or light blue symbols) and $30 \mu\text{m}$ (red or dark blue symbols).

in Nordrhein-Westfalen, Germany. We are also grateful to the Institute Jožef Stefan, Ljubljana, Slovenia during the irradiation for the support during neutron irradiations. The irradiation campaign has been supported by the H2020 project AIDA-2020, GA no. 654168. The beam test measurements have also received support by the Turkish Atomic Energy Authority (TAEK) under the project grant no. 2018TAEK(CERN)A5.H6.F2-20. This research project has been supported by the Marie Skłodowska-Curie Innovative Training Network of the European Commission Horizon 2020 Programme under contract number 675587 “STREAM”.

References

- [1] ATLAS collaboration, *Technical design report for the ATLAS inner tracker pixel detector*, CERN-LHCC-2017-021, CERN, Geneva, Switzerland (2017) [ATLAS-TDR-030].
- [2] H. Pernegger et al., *First tests of a novel radiation hard CMOS sensor process for Depleted Monolithic Active Pixel Sensors*, 2017 *JINST* **12** P06008.
- [3] W. Snoeys et al., *A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance*, *Nucl. Instrum. Meth. A* **871** (2017) 90.
- [4] T. Wang et al., *Depleted fully monolithic CMOS pixel detectors using a column based readout architecture for the ATLAS inner tracker upgrade*, 2018 *JINST* **13** C03039 [arXiv:1710.00074].
- [5] G. Aglieri et al., *Monolithic active pixel sensor development for the upgrade of the ALICE inner tracking system*, 2013 *JINST* **8** C12041.
- [6] R. Cardella et al., *MALTA: an asynchronous readout CMOS monolithic pixel detector for the ATLAS High-Luminosity upgrade*, 2019 *JINST* **14** C06019.
- [7] I. Caicedo et al., *The Monopix chips: depleted monolithic active pixel sensors with a column-drain read-out architecture for the ATLAS inner tracker upgrade*, 2019 *JINST* **14** C06006 [arXiv:1902.03679].
- [8] M. Munker et al., *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance*, 2019 *JINST* **14** C05013 [arXiv:1903.10190].
- [9] S. Meroli, D. Passeri and L. Servoli, *Energy loss measurement for charged particles in very thin silicon layers*, 2011 *JINST* **6** P06013.
- [10] *Xilinx Virtex-7 FPGA VC707 evaluation kit webpage*, <https://www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html>.
- [11] C. Ghabrous Larrea et al., *IPbus: a flexible Ethernet-based control system for xTCA hardware*, 2015 *JINST* **10** C02019.
- [12] ATLAS collaboration, *Large scale software building with CMake in ATLAS*, *J. Phys. Conf. Ser.* **898** (2017) 072010.
- [13] M. Kiehn, *Proteus beam telescope reconstruction*, *Zenodo*, (2019).
- [14] C. Kleinwort, *General broken lines as advanced track fitting method*, *Nucl. Instrum. Meth. A* **673** (2012) 107 [arXiv:1201.4320].