A Model Based Fast Protection System for High Power RF Tube Amplifiers Used at the European XFEL Accelerator

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Abstract—The driving engine of the superconducting accelerator of the European X-ray Free-Electron Laser (XFEL) is a set of 27 Radio Frequency (RF) stations. Each of the underground RF stations consists of a multi-beam horizontal klystron that can provide up to 10 MW of power at 1.3 GHz. Klystrons are sensitive devices with a limited lifetime and a high mean time between failures. In real operation, the lifetime of the tube can be significantly reduced because of failures. The special fast protection Klystron Lifetime Management (KLM) system has been developed to minimize the influence of service conditions on the lifetime of klystrons. The main task of this system is to detect all events which can destroy the tube as quickly as possible, and switch off the driving RF signal or the High Voltage (HV). Detection of events is based on a comparison of the value of the real signal obtained at the system output with the value estimated on the basis of a high power RF amplifier model and input signals. The KLM system has been realized in Field Programmable Gate Array (FPGA) and implemented in XFEL. Implementation is based on the standard Low Level RF (LLRF) Micro Tele-communications Computing Architecture (MTCA.4 or xTCA).

The main part of the paper focuses on an estimation of the klystron model and the implementation of KLM in FPGA. The results of the performance of the KLM system will also be presented.

Index Terms—DESY, European XFEL, control systems, protection systems, model estimation, MTCA, FPGA, klystron

I. INTRODUCTION

THE klystron is a high power RF amplifier. It is a specialized linear-beam vacuum tube. The RF system of the European X-Ray Free Electron Laser (XFEL) [1] consists of 27 RF stations that provide RF power at 1.3 GHz for the superconducting cavities. Each station consist of a Multi Beam Klystron (MBK) that can produce 10 MW of power at 1.3 GHz with the repetition rate of 10 Hz and the RF pulse

length of 1.5 ms. These stations are very expensive devices. The XFEL should work continuously over for 20 years with only a one day break per month for maintenance. In order to meet such demanding requirements, the lifetime of the tube should last in excess of 60 000 hours. Such a long lifetime is not always easy to achieve. Another problem is the stability of work of the klystron. In the case of the Free Electron Laser in Hamburg (FLASH) accelerator in DESY [2], 40% to 50% of the accelerator downtime is caused by klystrons and modulators [3]. Detection of events in MBK and reaction to them is a key in reducing the failure time.

There are a few factors which can reduce the lifetime and decrease the stability of the tube. Some of the main are:

- RF breakdowns (may damage the cavity surface and can pollute the RF window, which increases the reflected power);
- High RF reflections due to a breakdown somewhere in the waveguide system (may lead to beam loss);
- Work in deep saturation (may lead to beam loss and bad vacuum);
- Gun arc (damages the cathode and anode surfaces and can pollute the HV insulator and the cathode);
- High vacuum level in the tube (can cause RF breakdown in one of the klystron cavities or HV breakdown in the gun area of the klystron).

To prevent the occurrence of these destructive factors, a fast interlock is required. The KLM, developed at DESY, is precisely such a fast interlock and measurement system. The main task of this system is to monitor signals available from klystrons and react when the klystron parameters are over the permissible values. It is done mainly by comparing measured values with values estimated from the model. When the difference between the measured and estimated value reaches a set threshold, an error is reported. The occurrence of such an event is indicated by the interlock signal that switches off the klystron drive signal. In order to prevent any potential damage of the klystron, the system should react as fast as possible.

The KLM protection system was integrated with the LLRF system for XFEL [4]. It was implemented in the MTCA.4 architecture. Its current version uses the same components as the LLRF system. All algorithms for model estimation were implemented in FPGA. Almost all tests and measurements of the system were carried out on the klystron test stand, where klystrons have been tested before installation at the XFEL

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II. SYSTEM OVERVIEW

There are 6 RF and 4 analog signals available from each klystron. Two of the RF signals are the forward and reflected power signals from the directional coupler (DC) installed between the output of the preamplifier and the klystron input cavity. The other four RF signals are the forward and reflected power from high power DCs installed in each of the klystron's arms. Two of the analog signals are the klystron cathode voltage and cathode current waveforms obtained from the capacitive HV divider and the Rogowski coil respectively. Both of them are installed near the klystron gun, inside of the connection module. These two signals are used for measuring the real saturated klystron power, the long time klystron cathode emission and the partial discharge levels in the HV system. The third of the analog signals is the value of the current in one of the high voltage Power Supply (PS) units for the klystron vacuum pumps. The last of the analog signals is the sum of two output signals of the light spark detectors installed near the klystron output windows. RF signals are used mainly for the detection of events. All available signals are connected to KLM, and KLM has only one output signal that controls the RF gate. The diagram of the klystron with connected signals is presented in Fig. 1.

In general, the XFEL LLRF crate consist of: 6 pairs of down-converter and digitizer boards for the detection of a field in the cavities, a main controller with the vector modulator for the up conversion and generation of the drive signal, the CPU for the front end application and high level control, a timing board for providing a trigger, the master protection system (MPS) and one KLM pair. The vector modulator has an RF

The diagram illustrates the MTCA.4 LLRF system architecture. A central backplane (yellow bar) connects three main components: CPU and Timing (green blocks on the left), and three LLRF modules (LLRF CNTRL, KLM, and LLRF FD) on the right. The backplane carries PCIe, triggers, and clock signals. The LLRF modules are interconnected via an interlock (red line) and share clock signals (CLK). The LLRF CNTRL module (green) contains an FPGA with blocks FF, VS, FB, and SP. The KLM module (red) contains an FPGA with blocks ERR, AMP, FILT, and MODEL. The LLRF FD module (green) contains an FPGA with blocks +, IO, ROT, and FILT. The LLRF CNTRL module is connected to the KLM module via an interlock and clock signals. The KLM module is connected to the LLRF FD module via an interlock and clock signals. The LLRF CNTRL module is also connected to the KLM module via an interlock and clock signals. The LLRF CNTRL module is connected to the KLM module via an interlock and clock signals. The LLRF CNTRL module is connected to the KLM module via an interlock and clock signals.

The RF 1.3 GHz signals from the klystron are down-converted in RTM to an intermediate frequency (IF) of 54 MHz. Next, together with the DC signals, the IF signals are sent to the digitizer board, where they are sampled at 81 MHz. Digitized signals are processed in FPGA on an SIS8300L [6] digitizer board. If an event is detected, an error (interlock) signal is generated. In consequence, the RF driving signal is switched off. The block diagram of LLRF crate integrated with KLM is shown in Fig. 2.

The protection functions are determined on the basis of available signals from the klystron. They are:

- Protection functions can be written in the form of simple equations.

The reflection amplitudes at the input (A_{Rin}) and outputs (A_{R1}, A_{R2}) of the klystron are checked, and if they exceed the threshold values, an error will appear. The error conditions are:

$$A_{R1} \geq A_{R1LIM}$$

$$\begin{aligned} A_{R2} &\geq A_{R2LIM} \\ A_{Rin} &\geq A_{RinLIM} \end{aligned} \quad (1)$$

where A_{R1LIM} , A_{R2LIM} , A_{RinLIM} are limit values for reflection amplitudes.

The limiting levels are related to the maximum allowed Voltage Standing Wave Ratio (VSWR) on the corresponding channel and are defined as functions of the forward amplitude (A_{Fx}):

$$A_{RxLIM} = f(A_{Fx}) \quad (2)$$

B. Forward Check

The forward amplitude at the klystron output is checked and compared with its expected value. If the difference exceeds a protection level, the error will appear:

$$A_{OEXP} - A_{OVS} \geq A_{FLIM} \quad (3)$$

where A_{FLIM} is the maximum allowed difference between the expected and measured amplitudes, A_{OVS} is the sum of the output amplitudes at arm one (A_{F1}) and arm two (A_{F2}) of the klystron, normalized by coefficient 1/2:

$$A_{OVS} = \frac{A_{F1} + A_{F2}}{2} \quad (4)$$

The expected amplitude (A_{OEXP}) is a function of the input amplitude (A_{in}) and the klystron high voltage (U_H):

$$A_{OEXP} = f(A_{in}, U_H) \quad (5)$$

Protection against work in deep saturation is ensured by reporting too high input amplitude:

$$A_{in} \geq A_{SAT} \quad (6)$$

where A_{SAT} is the input amplitude value for which the klystron starts working in deep saturation.

IV. KLYSTRON MODEL

Klystrons are highly nonlinear devices. An adequate model of the klystron is required for a calculation of the expected forward amplitude at the klystron output (3, 5) and for the estimation of the maximum of the reflected wave amplitude (2).

A. Reflection Amplitudes

The reflection wave appears when the transmission line has a different impedance than the klystron impedance. During normal stable work the impedance at the klystron's input and outputs should not change. Maximum reflection can be calculated from the reflection coefficient defined as:

$$\Gamma = \frac{V_{ref}}{V_{for}} = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (7)$$

where V_{ref} is the reflection voltage, V_{for} is the forward voltage, Z_L is the load impedance and Z_0 is the source impedance.

At the klystron output, Z_L is the waveguide impedance and Z_0 is the klystron impedance. The waveguide impedance may change due to the RF breakdown in the waveguide system. The breakdown may be represented as a short circuit, for which $Z_L \cong 0$ and from (7) $V_{ref} \cong -V_{for}$.

Fig. 3. Reflected amplitude in function of forward amplitude at klystron output (top) and input (bottom) for different klystron voltages

At the klystron input, Z_0 is the preamplifier impedance and Z_L is the total input cavity impedance, which depends on the cavity and beam impedance [7]. This means that disturbance or lack of the beam causes change in the input impedance and results in an increase of the reflected power.

From (7) we can see that the reflection voltage is proportional to the forward voltage. The results of experiments confirmed that for stable operations at the klystron output and input the reflection amplitude is approximately a linear function of the forward amplitude (Fig. 3).

The function of the reflection limit can be defined as follows:

$$A_{RxLIM} = f(A_{Fx}) = a \cdot A_{Fx} + b \quad (8)$$

where a is the reflection coefficient and b is an offset for a given protection level.

B. Expected Forward Output Amplitude

The MBK amplitude to amplitude (AM/AM) conversion can be characterized by the modified Rapp's model that models amplitude distortions but no phase distortions. The Rapp's model can be used for systems that behave linearly up to the saturation point [8]. It uses three main parameters: saturation amplitude (p_0), signal gain of the amplifier (p_1), and parameter (p_n) that controls smoothness of transition from the linear to nonlinear region. The general expression describing AM/AM conversion of the klystron for a constant voltage, with additional coefficients (p_2, p_3) that define a drop in the over-saturation region, is as follows [9]:

$$A_{OEXP} = \frac{p_1 \cdot A_{in} + p_2}{\left[1 + \left(\frac{A_{in}}{p_0}\right)^{p_n}\right]^{1/p_n}} + p_3 \quad (9)$$

The characteristics of MBK and the fitted model for one klystron voltage are presented in Fig. 4. The maximum input and output amplitudes are normalized to 1.

Measurements for various voltages show that parameters p_1 and p_2, p_3 change approximately linearly with the measured voltage in the operating point range (see Fig. 5). In our case there is no output offset and for $A_{in} = 0$, $A_{OEXP} = 0$, $p_3 = -p_2$.

Fig. 4. Klystron input to output characteristic curve for one assumed voltage; voltage set on PS: 9200 V; measured and fitted curves, $p_0 = 0.48$, $p_1 = 1.568$, $p_2 = 0.008$, $p_n = 2.7$; norm of the residual $R_{ss} = 1.5e-4$, $R^2 \approx 1$

Fig. 5. Parameters p_i in function of voltage set on PS

Taking into account all relations, the following formula for the estimation of the output amplitude can be used:

$$A_{OEXP} = f(A_{in}, U_H) = \frac{p_1 \cdot A_{in} \cdot U_H + p_2 \cdot A_{in} + p_3 \cdot U_H + p_4}{\left[1 + \left(\frac{A_{in}}{p_0}\right)^{p_n}\right]^{1/p_n}} - p_3 \cdot U_H - p_4 \quad (10)$$

Model parameters p_i are estimated according to the measured characteristics of the klystron. For the best possible fitting it is required to run the klystron scan for a minimum of three different voltages. The klystron scan is a set of measured values of the input amplitude, the sum of the output amplitudes and the voltage for various input amplitudes in the range from zero to the saturation point. All values are normalized to 1, where 1 means the maximum possible measured value on ADC.

Fitting of parameters p_i in (10) is realized by solving the problem of the nonlinear least-squares curve fitting. In order to obtain an optimal solution to this problem a definition of a starting point for the fitting function is required. In our case, we estimate parameters p_i for the linear part of the characteristic, which leads to solution of the following simple linear equation:

$$A_{OEXP} = p_1 \cdot A_{in} \cdot U_H + p_2 \cdot A_{in} + p_3 \cdot U_H + p_4 \quad (11)$$

The fitted model based on measurements for three various voltages and its comparison with real signals is presented in Fig. 6.

Fig. 6. Transfer curves of THALES TH1802 MBK for 5 various power supply voltages; parameters estimated using a set of 3 voltages: 8800 V (-0.31a.u.), 9100 V (-0.32a.u.), 9400 V (-0.33a.u.); $p_0 = 0.45$, $p_1 = -9.12$, $p_2 = -1.17$, $p_3 = -2.076$, $p_4 = -0.42$, $p_n = 2.67$; norm of the residual $R_{ss} = 3.5e-3$, $R^2 = 0.995$

Fig. 7. Relative percentage error between the estimated amplitude calculated from the approximated model and the measured values in function of the input amplitude for various voltages.

The parameters of the model were estimated for three klystrons and for 20 various operating voltages for each one. Experiments have shown that in some ranges the model fits better than in others. For higher voltages there appear nonlinearities that are not included in the model. For lower voltages the parameters also do not change exactly linearly with the voltage (Fig. 5). For this reason it is difficult to fit parameters so as to ensure a constant error level in the entire range of voltages. Therefore it is important to select proper voltages enabling the estimation of the parameters with an acceptable error in the operating voltage range. The relative error between the estimated amplitude calculated from the approximated model and the measured values in the function of the input amplitude is presented in Fig. 7. As we can see, the maximum relative error is smaller than 2% of the amplitude level for all voltages. This error level determines a minimum protection threshold for detection of events and is acceptable for the system.

V. FPGA IMPLEMENTATION

In modern control systems, FPGAs are used to process digital signals. They create the possibility to implement sophisticated algorithms with minimal latency and high data throughput.

This section will describe the blocks used for the detection of events. All algorithms have been implemented in FPGA and were optimized for lower latency. Current implementation is done on an SIS8300L board Virtex6 (xc6vlx130t) FPGA

chip. All calculations are pipelined. The dedicated Xilinx DSP48E1 slices [10] were used to perform additions and multiplications in the algorithm implementation. The arithmetic is done using fixed point number representation in the format: $s:m:f$ where s represents the number of sign bit, m the number of integer bits and f the number of fractional bits. The detection of events is divided into a few main blocks, which are presented in Fig. 8.

Fig. 8. Top block diagram of FPGA implementation for detection of events divided into blocks: field detection, low pass filters (LPF), model estimation and error detection

A. Field detection

For field detection the non-IQ digital demodulation is used [11]. From the I and Q signals, the amplitude can be calculated using the CORDIC algorithm. Such a solution is characterized by high precision but also high latency. To reduce delay, the amplitude (A) of the signal is calculated in two steps. First we calculate the square of the amplitude using I and Q components, and next we estimate the square root of this value applying interpolation:

$$\begin{aligned} A^2 &= I^2 + Q^2 \\ A &= \sqrt{A^2} \end{aligned} \quad (12)$$

In our system, the sampling frequency (FS) equals 81 MHz and the internal frequency (IF) 54 MHz. For this IF and FS frequencies the fastest way to calculate samples of the square of the amplitude is to use the formula [12]:

$$A_{[n]}^2 = (2 \cdot x_{[n-2]} \cdot x_{[n-1]} - x_{[n]}^2) + 3 \cdot (x_{[n-1]}^2 - x_{[n]}^2) \quad (13)$$

where $x_{[n-2]}$, $x_{[n-1]}$, $x_{[n]}$ are consecutive samples of the ADC output. The input ADC data have 16 bits. Three clock cycles are required to calculate 32 bit number representing the square of the amplitude.

The square root is estimated using the linear interpolation of the square root function that is implemented on two Look-Up-Tables (LUT). The interpolator is given by the formula:

$$A = a(x_q) \cdot (A^2 - x_q) + b(x_q) \quad (14)$$

where $a(x_q) = \Delta\sqrt{x_q}/\Delta x_q$ and $b(x_q) = \sqrt{x_q}$ are parameters of function of the discrete variable $\sqrt{x_q}$, where x_q is the amplitude, and are given by LUT. Choosing a large number of interpolation points we can reduce the error but it requires bigger tables and more resources, which can be a limiting factor. A compromise between the error value and available resources has to be taken. In Fig. 9, the relationship between the percentage errors of calculations and the number of interpolation points is illustrated. We can observe that we obtain the biggest errors for small amplitudes. This limits the operating range for really small amplitudes. To reduce the possibility of false alarms a proper adjustment of the signal level to the operatin range is required.

Fig. 9. Interpolation errors of square root function of A^2 for various numbers N of interpolation points

Fig. 10. Block diagram of amplitude detector

Each RF signal has a dedicated field detection module. Calculations of the amplitude are carried out in parallel for all channels. There are six modules in total. The block diagram of the amplitude detector is shown in Fig. 10.

B. Filters

The klystron bandwidth equals 6 MHz and is smaller than the bandwidth of sampled data that equals 41 MHz. To reduce noise and avoid detection of false alarms it is necessary to apply low pass filters. For reasons of low latency, they have been implemented as a simple moving average over four samples. For all signals the same filter defined by the formula:

$$A_{av}[n] = (A_{[n-3]} + A_{[n-2]} + A_{[n-1]} + A_{[n]})/4, \quad (13)$$

has been applied, where $A_{[n-3]}$, $A_{[n-2]}$, $A_{[n-1]}$, $A_{[n]}$ are successive amplitude samples.

C. Online Model Estimation

The estimation of the model is based on relatively complex formula (10). In FPGAs, calculation of divisions and powers is difficult to implement and very time-consuming. In applications requiring low latency this creates an essential problem. To overcome these difficulties it is much more suitable to interpolate some specified part of formula (10). Calculations are then much faster, and the interpolation error does not affect the whole estimation error significantly. For the aims of implementation, formula (10) can be written in the form:

$$A_{OEXP} = I \cdot (p_1 \cdot A_{in} \cdot U_H + p_2 \cdot A_{in} + p_3 \cdot U_H + p_4) - (p_3 \cdot U_H + p_4)$$

where I denotes a linear interpolator of function:

$$f(A_{in}) = \frac{1}{\left[1 + \left(\frac{A_{in}}{p_0}\right)^{p_n}\right]^{1/p_n}}$$

The block diagram for the calculation of the estimated amplitude is presented in Fig. 11. The precision of multiplications is 18 bits times 25 bits, and the precision of adders is 25 bits. The precision of operation is determined by one DSP48 slice. Data are represented as fixed point numbers. The voltage is a 16 bit number interpreted as 1:0:15, the input amplitude is an 18 bit number interpreted as 1:0:17 and the parameters are 25 bit numbers interpreted as 1:4:20. After every multiplication all numbers are converted to the format 1:4:20, and finally the estimated amplitude is converted to the format 1:0:17.

The linear interpolator I of function $f(A_{in})$ is realized in the same way as the interpolator of the square root for the field detection module. Only the contents of the LUTs are different. The interpolation is given by formula (14), where $a(x_q) = \Delta f(x_q)/\Delta x_q$ and $b(x_q) = f(x_q)$ are parameters of function of the discrete variable x_q . For interpolation of function $f(A_{in})$ 512 interpolation points were selected as optimal. The block diagram of the interpolator is presented in Fig. 12. The relative percentage error of calculations of the estimated amplitude for various numbers of interpolation points is presented in Fig. 13.

Fig. 11. Block diagram of FPGA implementation for amplitude estimation

Fig. 12. Interpolator I with 512 interpolation points

Fig. 13. Relative percentage error of FPGA output amplitude estimation for various numbers of interpolation points

D. Error Detection

The error detection module is implemented as a set of 18bit comparators that implement inequalities (1), (3), and (6). The results of comparison are latched and kept till the next pulse.

E. Delay Estimation

The total delay of the digital part of the system can be estimated taking into account implementation details. It is estimated to be around 380 ns. The delay of particular modules and the total delay of the FPGA and digital parts is provided in table 1.

TABLE I
ESTIMATION OF DELAY

Module name	clock cycles	time
ADC (SIS8300L)	14	168 ns
Amplitude detection	6	72 ns
Filter	1	12 ns
Model Estimation	6	72 ns
Error detection	2	24 ns
RF gate		30 ns
FPGA total	15	180 ns
Digital total		378 ns

VI. RESULTS

In this section, the examples of errors detected by the system are discussed. The verification of implementation and measurements of the klystrons was performed on the specialized klystron test stand. Events are from the MBK TH1802 produced by Thales.

A. Online Model Estimation

The verification of online model calculations was carried out by comparing the estimated amplitude with the sum of the forward output amplitudes during RF pulse. Tests were performed for various voltages and various levels of the input amplitude. Measured and estimated amplitudes obtained during the stable operation are presented in Fig. 14.

Fig. 14. Measured and estimated klystron output amplitudes during RF pulse

Fig. 15. Relative percentage error between estimated and measured amplitude at the klystron output for various operating points during a normal operation with no event and during the RF breakdown event

Many experiments show that in specific operation ranges the klystron can manifest nonlinearities that are not included in the model. Nevertheless, differences between values estimated on the basis of the model and measured values do not exceed 2%. This is fully acceptable for the protection system. The errors of the output amplitude for various klystron operating points, also during detected events, are presented in Fig. 15.

B. Event Detection

During the operation of the klystron a number of events were identified. When an event is detected all data are stored on the hard drive for further analysis. There are three main types of events: RF breakdown (Fig. 16), high reflection at the output (Fig. 17) and high reflection at the input (Fig. 18). Point 0 on the time axis denotes the instant when an event was detected in FPGA, and the RF driving signal was switched off.

Fig. 16. Amplitude curves for all RF signals during RF breakdown event

Fig. 17. Amplitude curves for all RF signals during high reflection at the output

Fig. 18. Amplitude curves for all RF signals during high reflection at the input

C. Reaction Time

The reaction time on events is one of the most important parameters for each fast interlock system. In order to calculate the delay of the digital loop in our system, the delay time was estimated and then measured. From an event at the ADC input to the signal on the interlock line about 400 ns elapse. When we take into account all analog components of the system, cables, mixers and the amplifier, the total reaction time is about 500-600 ns. The total delay can be estimated from the amplitude curves demonstrated in Fig. 16-18. For example, in Fig. 16 we can observe that the event occurs around 200 ns before it was detected in FPGA. The RF drive (forward in) signal is switched off around 300 ns after its detection. This gives around 500 ns of total delay.

VII. SUMMARY

In this paper, the protection and measurement KLM system for klystrons was presented. The system was successfully implemented and integrated with the LLRF system. Its implementation was tested on the specialized klystron test stand. The mathematical formulas for the protection system and the klystron model estimation were derived. The signal processing architecture was also described. The KLM system can properly detect various kinds of error events: RF breakdown as well as a high reflection power at the output and input. The experiments confirmed that the KLM system reacts properly to all events, and switches off the RF drive signal with a delay of around 500 ns.

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