Thermal and hydrodynamic studies for micro-channel cooling for large area silicon sensors in high energy physics experiments

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Abstract

Micro-channel cooling initially aiming at small-sized high-power integrated circuits is being transferred to the field of high energy physics. Today's prospects of micro-fabricating silicon opens a door to a more direct cooling of detector modules. The challenge in high energy physics is to save material in the detector construction and to cool large areas. In this paper, we are investigating micro-channel cooling as a candidate for a future cooling system for silicon detectors in a generic research and development approach. The work presented in this paper includes the production and the hydrodynamic and thermal testing of a micro-channel equipped prototype optimized to achieve a homogeneous flow distribution. Furthermore, the device was simulated using finite element methods.

Keywords: micro-channel, cooling, HEP, silicon sensors, ANSYS, CFX, OpenFoam, microfluidics, heat sink, DESY, IMB-CNM, heat

1. Introduction

As electronic devices are becoming smaller and smaller their power density is increasing and cooling becomes more important than ever before. The small dimensions of today's integrated circuits demand for a down scaling of heat sinks. The first cooling of electronics through micro-channel flows was accomplished in 1981 by Tuckerman and Pease [1]. The endeavor to achieve a better understanding of heat and mass transfer through micro-channels has led to an ever growing number of approaches. Using varying channel geometries, different fluids and multi-phase flows helped to increase the efficiency of micro-channel cooling and led to tailor-made solutions in various fields of applications [2].

The attractiveness of this technology to high energy physics (HEP) is less its capability to handle high power densities, but its potential to provide a direct and homogeneous cooling, to save material and to satisfy tight restrictions on the choice of materials, regarding radiation hardness and thermal expansion.

In HEP experiments like the ones of the LHC, the silicon detectors, which are positioned very close to the interaction point, receive considerable radiation doses. The sensors in tracking detectors, equipped with readout electronics, have to be kept at low temperatures around 0 °C and in some cases much less [3]. This is mainly to keep the leakage current - introduced by radiation damage - low and to avoid thermal runaway. The cooling system typically adds a significant amount of material to the detector, leading to multiple scattering of charged particle tracks and conversions of photons into electron-positron pairs when passing through the material.

Saving material is essential to maintaining a good momentum resolution especially for low momentum particles. To do so, the heat sinks for the sensors, the readout electronics and the rest of the detector have to be within a certain radiation length, to limit multiple scattering and conversions. Moreover, the difference of the coefficient of thermal expansion (CTE) between sensor and heat sink must be kept small to avoid mechanical stress occurring by undergoing temperature cycles during production, installation and operation.

The micro-channel system presented in this paper is built upon a channel array etched in silicon, closed with a Pyrex layer and operated with a single-phase hydro-fluoroether coolant [4]. Pyrex was chosen for the purpose of the studies presented here, because it provides the ability to visually inspect the channel array for impurities and empty channels. A design has been developed to maintain a homogeneous distribution of the coolant across the micro-channel layout. For thermal

characterization, heat was distributed homogeneously across the device. A design cooling mainly the parts exposed to a heat flow was already demonstrated in the ALICE ITS detector development [5] and a material reduction via thinning of the micro-channel device by the NA62 group [6].

Besides the ALICE and the NA62 experiment, also LHCb [7] developed a micro-channel cooling solution for their application. The approaches of these experiments are similar to the one used in the present work, but with different layouts and coolants. The LHCb micro-channel cooling system is based on an evaporative CO_2 coolant and a channel design adopted to that mode of operation. The NA62 experiment on the other hand utilizes also a single-phase perfluorocarbon coolant, but a different flow distributing method by using a double layout design with two inlets and two outlets, different channel sizes and manifold design. The ALICE experiment is based on a small area cooling design. This work is especially interested in the homogeneous distribution of the coolant across a large area to maintain small temperature gradients.

2. Layout and calculations

The layout of the micro-channel cooling device was designed to fit on a 4 inch wafer. To keep the pressure drop as low as possible, a design was chosen based on manifolds connecting a number of smaller channels. One inlet and one outlet oppositely arranged are then connected to a cooling circuit. To provide a homogeneous flow through all n channels, the pressure at each transition from manifold to smaller channel must be the same. From that assumption follows:

$$p_n = p_{n+1}, \tag{1}$$

with p_n the pressure in the manifold at the entrance to the n-th channel. The pressure must be adjusted by decreasing the width of the inlet manifold along the flow direction. The flow in the inlet manifold decreases with the number of channel entries along the way:

$$Q_n = Q_0 - n\frac{Q_0}{N}, \tag{2}$$

with Q_0 being the total flow through the device, N the total number of channels and Q_n the flow through the manifold at channel n. The pressure drop derived by the Navier-Stokes equation for a circular channel cross section is used as a good approximation:
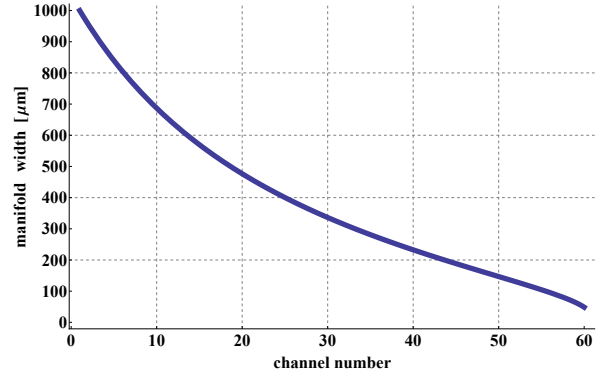
$$\Delta p = Q\frac{8\eta L}{\pi a^4}, \tag{3}$$

Figure 1: The width of the manifold according to equation 6, for 60 channels and a starting width of $1000\,\mu m$ at the first entry to a smaller channel.

with η the viscosity, L the overall channel length and a the characteristic dimension. The characteristic dimension of the manifold at channel n is given by a_m

$$a_m^4(n) = (1 - n\frac{1}{N})a_c^4 \tag{4}$$

with a_c the characteristic length of the manifold at the first channel entry. The characteristic length is chosen to be the hydraulic diameter which - in the case of a fully filled channel - is

$$a = 2 * \frac{w * h}{w + h}, \tag{5}$$

with h the channel height and w the width of the channel. The hydraulic diameter of the manifold at the entry to channel number n is $a_m(n)$. This results in the width of the manifold at channel n being

$$w_m(n) = \frac{h\left(-\frac{w_c^4 h^4(-1+n-N)}{(w_c+h)^4 N}\right)^{\frac{1}{4}}}{-h + \left(-\frac{w_c^4 h^4(-1+n-N)}{(w_c+h)^4 N}\right)^{\frac{1}{4}}} \tag{6}$$

with a total channel number of N. For technical reasons the manifold function was approximated by eleven linear sections.

For mechanical robustness of the $300\,\mu m$ to $500\,\mu m$ thick silicon wafer, the size of the channels was chosen to be $100\,\mu m \times 100\,\mu m$ with a starting width of the manifold $w_c = 1000\,\mu m$ at the first channel entry. The structure has 60 parallel channels from inlet to outlet manifolds, with a pitch of $675\,\mu m$. Figure 1 shows the shape of $w_m(n)$ for $n = 60$ channels and a starting width of $1000\,\mu m$. The channels were designed with a 15° angle with respect to the perpendicular of the manifolds in order to avoid possible flow separations and limit resulting recirculating flows [8]. Inlet and outlet holes to
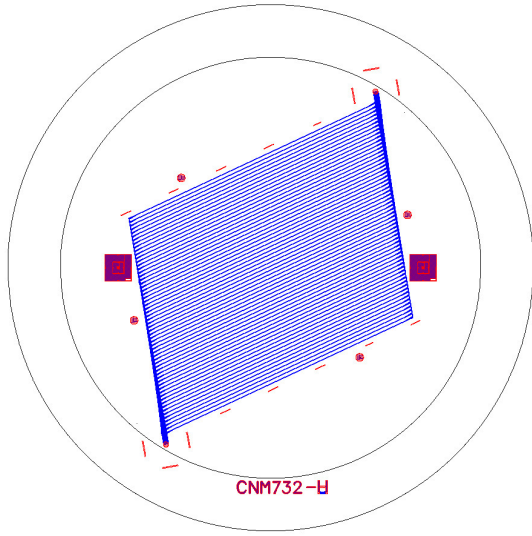
Figure 2: Layout of the micro-channels, projected on the outlines of a 4 inch wafer.
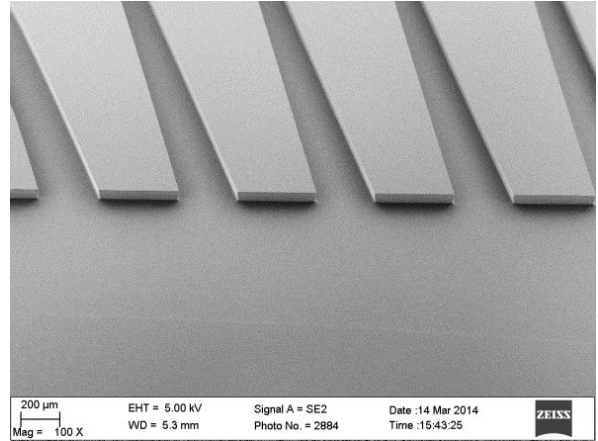

Figure 3: Electronic microscopy image of the channels produced by the DRIE process.
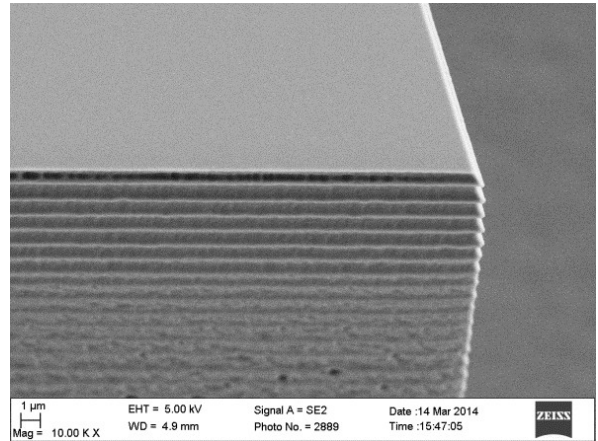

Figure 4: Detailed view of the scalloping effect at the micro-channel walls produced by DRIE process, note the smaller scale compared to figure 3.

the manifolds with 1 mm diameter were added. Finally the whole design was rotated by 10° with respect to the wafer axis to avoid coincidence of the channel etch direction with the silicon crystallographic planes, in order to avoid cracks or full wafer cleaving.

The channel ends were widened to prevent possible turbulence at sharp edges resulting in a structure shown in figure 2. Additional technical test structures, and alignment marks were added to facilitate processing.

3. Fabrication

The fabrication of the micro-channel assembly structure was performed in the clean room of the Centro Nacional de Microelectronica (IMB-CNM, CSIC), Barcelona, Spain. The assembly was performed in two steps. In the first step, a silicon wafer was micromachined by Deep Reactive Ion Etching (DRIE) in order to create the channels and the inlet and outlet in the silicon. In the second step, the micro-machined silicon wafer was bonded by an anodic process to a blank Pyrex wafer in order to seal the micro-channels and define the cooling structure inside the assembly.

As shown in figure 7, the process starts with a blank 4 inch diameter, 300 μm to 500 μm thick, double-side polished silicon wafer. After a standard cleaning of the wafer, the layout previously defined was transferred to the wafer by a photo-lithography process. The photolithographic resist was used as mask during the following silicon etching process. Then, a 100 μm etch was

processed with an ALCATEL 601-E equipment. The etching was carried out by the Bosch process based on consecutive steps of silicon plasma etch and deposition of a passivation layer which protects the silicon walls, achieving in this way a very anisotropic etching and a high aspect ratio of the micro-channels [9] [10]. A Scanning Electron Microscopy (SEM) picture of the result of this etch and details of the resulting micro-channels can be seen in figure 3 and 4 where the characteristic rippled structure (scalloping) of the DRIE can be seen in the micro-channel walls.

After the micro-channels were created in one side of the wafer, a thermal oxide was grown at both wafer sides to protect the micro-channels from the next etching process. A metal mask was defined on the back side of the wafer by a second photolithographic step, leaving open
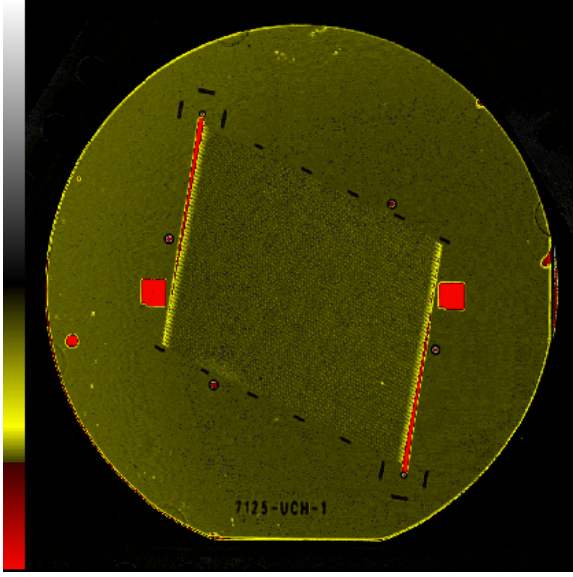
Figure 5: Scanning Acoustic Microscopy image of the assembly produced by anodic bonding.

Figure 6: Optical image of the resulting assembly. The four white dots around the channel structure are alignment marks.

the areas that have to be etched from the back side. This mask has to be aligned with the micro-channels at the other side of the wafer (double-sided alignment). The silicon oxide layer previously grown was then etched by a physical dry process in the open areas not covered with metal, and later the second DRIE etch was performed on the same open areas. In this process, the etching continues for the whole silicon thickness, creating through holes to define the inlet and outlet entries to the micro-channels. Finally, the metal mask was removed, the protecting oxide was wet etched, and a deep cleaning (RCA clean) was performed on the wafer to leave the bare silicon exposed for the next step.

In the second step of the assembly fabrication, a blank Pyrex wafer, 500 µm thick, was used to close the micro-channels created in the silicon wafer by an anodic bonding process [11] [12]. The equipment used was a SÜSS MicroTec SB6e. For the anodic bonding a high potential difference (1000 V) was applied between the two wafers which are in close contact. The high electric field across the wafers enhances the ion interchange needed to form the Si-SiO_2 bonding with a relatively low temperature ($< 400\,°C$). The process creates a strong bond between the two wafers sealing the micro-channels.

The assembly was then analyzed by Scanning Acoustic Microscopy (SAM) with a Sonoscan GEN-5 equipment, which detects any voids between the wafers, to test the bond quality. An example of the SAM results can be seen in figure 5. The micro-channels sealed in
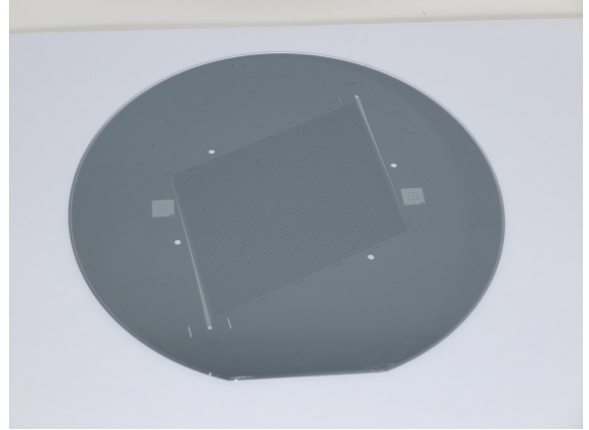
the interior of the assembly can be clearly identified together with the alignment marks besides them. Only a small negligible void, recognizable as red dot in figure 5, can be seen at the very left edge far away from the micro-channels, probably due to some small particle on either of the two wafers before the process. In figure 6 an optical image of the assembly can be seen where the micro-channels are visible through the transparent Pyrex wafer that seals them.

4. Simulation

4.1. Simulation environment

Simulations are useful to study effects on the measurements due to changes in the setup such as using a different fluid, different boundary conditions, or can simply help to provide an understanding of a malfunctioning device.

The interFoam solver of the open source computational fluid dynamics software OpenFoam [13] was used to simulate the initial filling process of the micro-channels in a multi-phase approach. Furthermore the CFX package of the numeric simulation software ANSYS [14] was used to build a 3d model to calculate flow and thermal properties of the micro-channel device in a single-phase approach. The layer structure of the micro-channel walls as visible in figure 4 was not implemented in the simulation. The surrounding atmosphere was neglected as well, which means that there is no heat transfer through the wafer surface to the outside. Thermal properties were simulated modeling the channels in the silicon, closed with a Pyrex layer and ports attached to the inlet and the outlet.
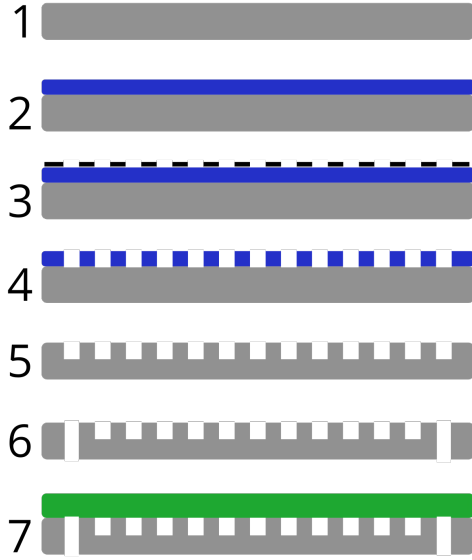
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Figure 7: The basic steps of micro-channel fabrication. One side of blank wafer (1) is coated with a photo-lithographic resist (2). A mask of the layout is used (3) to transfer the channel design to the resist (4). The 100 μm deep channels are etched into the silicon (5), the inlet and outlet holes are added (6) and closed with a Pyrex layer (7).

The simulation of the above setup included flow calculations as well as thermal calculations, thus the mesh can be split into a fluid volume and a solid volume with different requirements. The volumes representing the fluid demand a much finer granularity than the solid parts which play only a role for the thermal calculations. An overall element size of 10 μm to 30 μm was chosen along the cross section of the smaller channels and an element size of 800 μm along the channel length. The overall element size of the manifolds was kept between 20 μm and 70 μm. Three to four mesh layers were placed on all fluid boundary walls with a starting thickness of 2 μm and a growth rate of 1.2. The solid compartments were meshed coarser, with element sizes ranging from 800 μm for the wafer bulk material, down to 100 μm at contact surfaces. This resulted in models with a number of elements ranging from a few million to over twenty million. The properties of the fluid in the simulation are kept close to the one in the experiment, with a density of around 1500 kg m^{-3}, and a dynamic viscosity of 0.58 g m^{-1} s^{-1} at around 20 °C. Because the maximum fluid velocity in the simulation was found to be around 3 m s^{-1}, resulting in a maximum Reynolds number of around 1100, a laminar fluid model was chosen for the calculations.
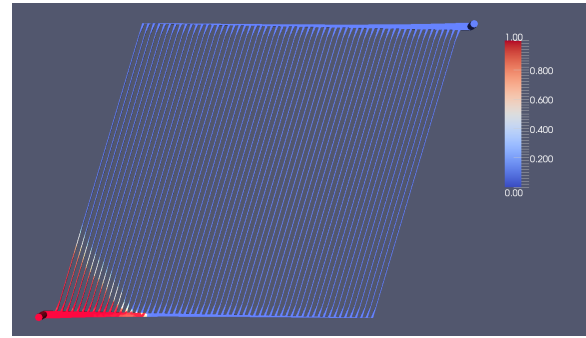
(a)
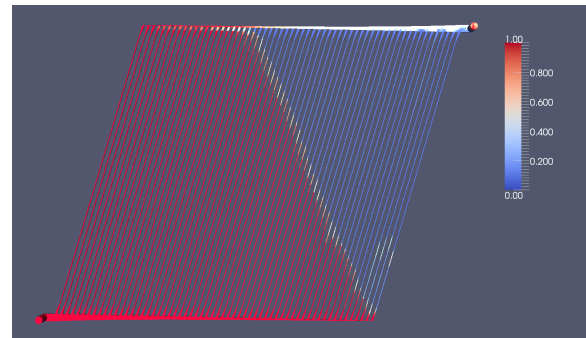
(b)
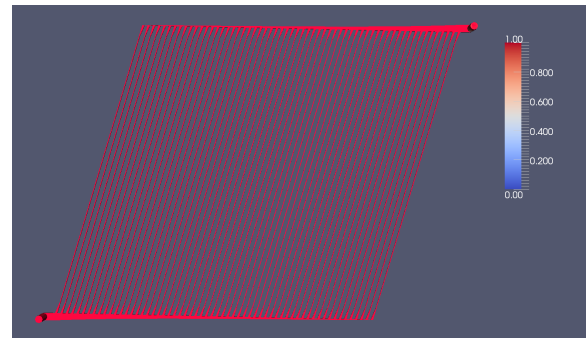
(c)

Figure 8: The initial filling of the micro-channels simulated with OpenFoam. The red colored phase represents the fluid and the blue phase the air. The pressure was increased over time from 0.1 bar to 0.5 bar, resulting in a flow rate of around 1 ml min^{-1} to 5 ml min^{-1}. Figure a) shows the filling process after 0.06 s, figure b) after 2.19 s and c) after 6 s.

4.2. Simulation results

Results of the simulated filling process are shown in figure 8. They show a good agreement with the behavior observed in the experiment by filming the filling process through the Pyrex. The homogeneous distribution of the fluid is very important to avoid dryouts due to insufficient flow in certain regions or empty channels due to air enclosures at channel entries, creating clogging [15],

Table 1: Calculated pressure values p from the simulation of flow rates Q between $4\,\mathrm{ml\,min^{-1}}$ and $40\,\mathrm{ml\,s^{-1}}$.

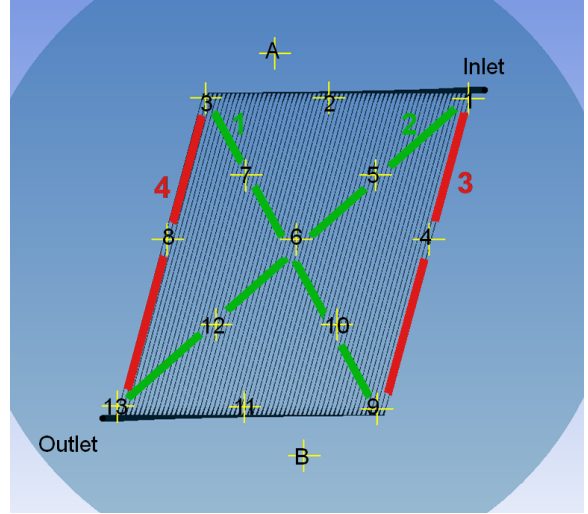| Q [ml min^{-1}]	p [bar]	Q [ml min^{-1}]	p [bar]
4	0.5	24	4.3
8	1.1	28	5.3
12	1.8	32	6.4
16	2.6	36	7.9
20	3.4	40	9.1
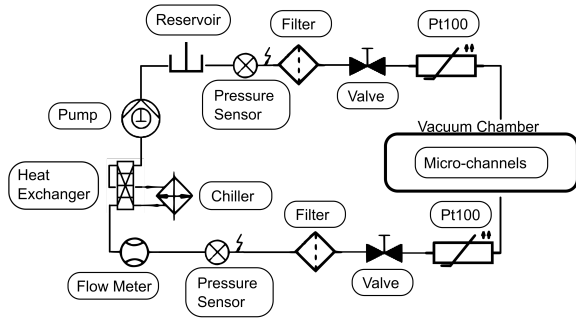
Figure 9: Sketch of the setup.

Figure 10: Pt100 temperature dependent resistors placed on the silicon surface.

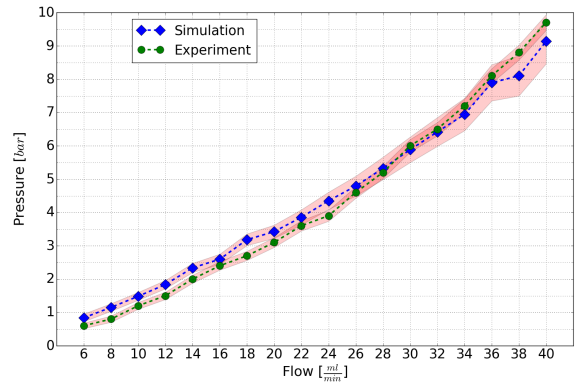Figure 11: Pressure versus flow comparison between simulation and experiment.

which can lead to additional pressure drops or complete malfunction.

Flow characteristics were calculated in the range of $10\,\mathrm{ml\,min^{-1}}$ to $40\,\mathrm{ml\,min^{-1}}$ with the flow properties of hydrofluoroether (HFE) [4]. The results in table 1 show the pressure p calculated at the inlet for a given flow rate Q.

After simulating the flow, the thermal properties of the solids were added to the simulation. The inlet temperature was set to $19\,°\mathrm{C}$. As mentioned previously, the convective and radiative heat transfer to the environment was not implemented in the simulation, thus the effective heat flux through the wafer differed from the experiment. The results of the thermal study are presented together with the experimental results in section 5.2.

5. Measurements

5.1. Experimental setup

The schematics of the setup are shown in figure 9. The setup is built around a high pressure liquid chromatography pump (HPLC) [16] aimed at low flow applications providing a maximum flow rate of $300\,\mathrm{ml\,min^{-1}}$ and a maximum pressure of $70\,\mathrm{bar}$. A heat exchanger cooled by a cooling unit [17] is used to control the temperature of the coolant in the main circuit. To accurately measure flow characteristics like flow rate, tem-

perature and density, a flow meter [18] using the Coriolis method was set right behind the heat exchanger. Two pressure sensors [19] were used, one before and one after the micro-channel device, to measure the pressure drop through the channel array. The valves [20] and filters [21] used do not contribute noticeably to the measured pressure drop. All devices are connected via steel pipes with 1/8 inch outer diameter which are converted to steel pipes with 1/16 inch outer diameter to connect to the micro-channel inlet and outlet via NanoPort connectors [22]. The following measurements presented in this paper were carried out with the cooling unit cooling the fluid to approximately $19\,°\mathrm{C}$ at the inlet of the micro-channels and an environment temperature of around $21\,°\mathrm{C}$, and the wafer was not insulated or put in any controlled atmosphere.
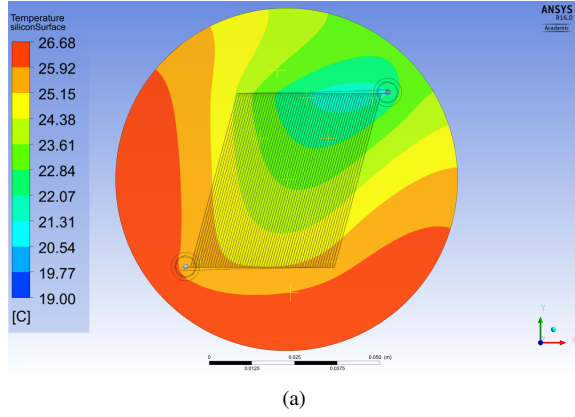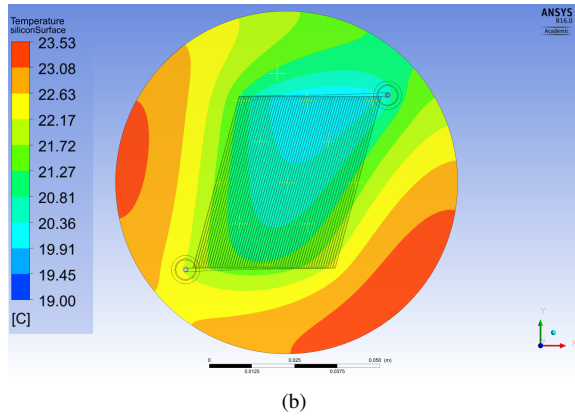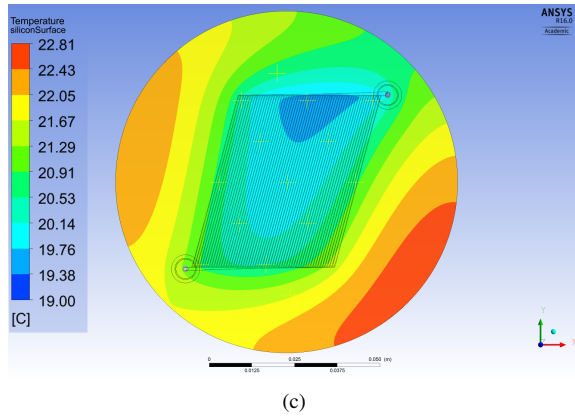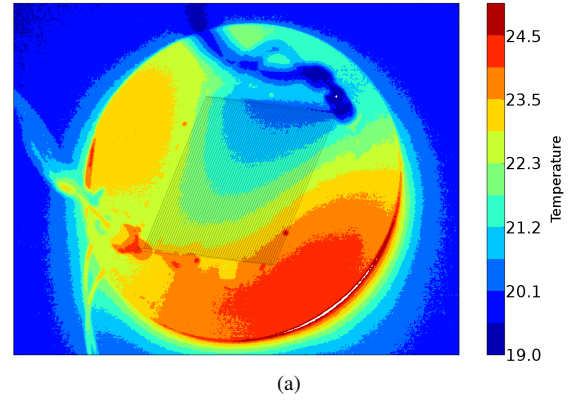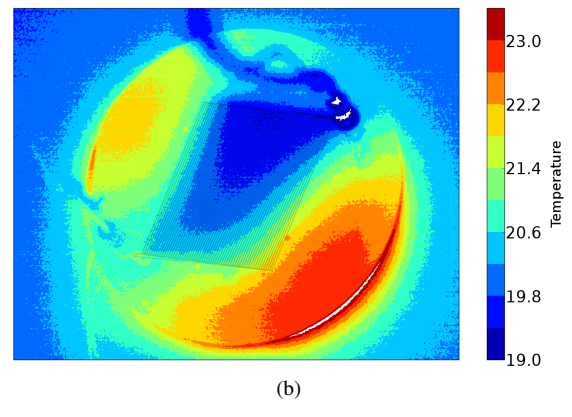
Figure 12: Simulated temperature maps of the silicon side of the micro-channel wafer, for 30.8 mW cm^{-2} and the superimposed channel structure. The fluid inlet is at the top right and the outlet is at the bottom left. (a) 10 ml min^{-1}, (b) 30 ml min^{-1}, (c) 50 ml min^{-1}.

Figure 13: Temperature maps of the silicon side of the micro-channel wafer taken with an infrared camera with the heater set to 30.8 mW cm^{-2} and the superimposed channel structure. (a) 10 ml min^{-1}, (b) 30 ml min^{-1}, (c) 50 ml min^{-1}.
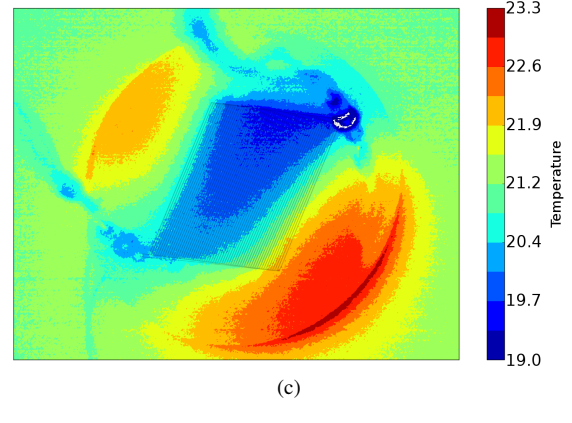
The most crucial measurements of thermal characteristics of a heat sink depend on the temperature difference of the coolant between the inlet and outlet. This value represents directly the heat transported out of the system by the coolant. For that reason two Pt100 temperature dependent resistors are placed on the pipes just at the entry and exit points of the micro-channel device.

To be flexible in terms of temperature range a hydro-fluoroether [4] was chosen as coolant due to its low viscosity at low temperatures (around 0.58 g m^{-1} s^{-1} at 20 °C).

For determining the thermal properties of the micro-channel device, the heat load was chosen to satisfy two main criteria. It provided a homogeneous heating and covered the whole wafer surface. For this purpose a 4 inch heater [23] was used, which has exactly the size of the full micro-channel wafer. To measure the temperature on the wafer surface, fifteen Pt100 resistors were placed on the silicon as shown in figure 10. In addition, an infrared camera [24] was used to map the temperature distribution across the whole wafer surface.

In a real detector the power will not be homogeneously distributed over the area to be cooled, but mainly across the readout electronics. This work presents a generic approach to test micro-channels as a cooling structure to transport heat out of a system and since the channel layout is not adapted to a specific detector design, the heat was distributed homogeneously across the wafer. The heater was set to $30.8\,\mathrm{mW\,cm^{-2}}$, $43.1\,\mathrm{mW\,cm^{-2}}$, $55.5\,\mathrm{mW\,cm^{-2}}$ and $67.8\,\mathrm{mW\,cm^{-2}}$, which corresponds to $2.5\,\mathrm{W}$, $3.5\,\mathrm{W}$, $4.5\,\mathrm{W}$ and $5.5\,\mathrm{W}$ over the full wafer surface. Running the setup at different heat loads can reveal the weak points of the layout or material composition. The following measurements were performed at an inlet temperature of around $19\,^{\circ}\mathrm{C}$ and flow rates ranged from $10\,\mathrm{ml\,min^{-1}}$ to $50\,\mathrm{ml\,min^{-1}}$ in $5\,\mathrm{ml\,min^{-1}}$ steps.

5.2. Experiment results

Figure 11 compares the fluid pressure at the inlet of the micro-channel structure versus the total flow through the device for both the simulations and the experiment. A possible explanation for the different slopes observed in the simulation and the measurement crossing each other at around $34\,\mathrm{ml\,min^{-1}}$ is the increased wall surface area, due to the scalloping mentioned in section 3. The increased surface area of the channel walls might increase the pressure drop at higher flow rates, which is missing in the simulation. Nevertheless, the simulated values are in a good overall agreement with the experiment. The mesh in the simulation was refined until the results did not improve anymore, and the only differences were fluctuations in the obtained pressure drop values. The fluctuations increased with higher flow rates and the error on the simulated data in figure 11 is based on these remaining fluctuations. The pulsations of the pump are causing a deviation of the desired flow rate. The uncertainty due to the precision of the pressure sensor is negligible in comparison to the error caused by the pulsations. The deviation from the preset flow rate is represented by the red error band surrounding the experimental measurement data points.

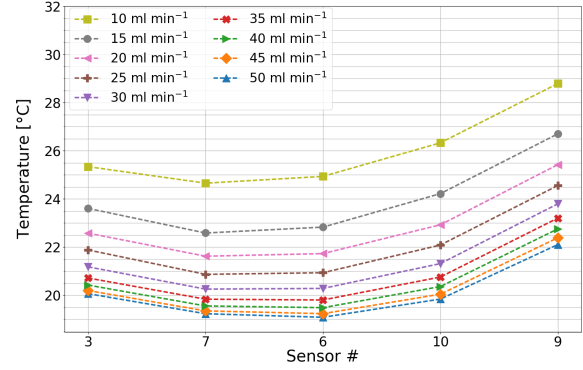Destructive tests were performed, showing that the

Figure 14: Temperature measured along line 1, as indicated in figure 10.

wafer broke near the inlet at a critical pressure of over 30 bar.

The temperature measurements obtained with the infrared camera were used primarily to study the temperature distribution across the wafer, whereas the Pt100 resistors were used to obtain precise measurements at certain points on the wafer. An offset measurement of all resistors at a fixed temperature was used to calibrate them to one reference resistor. The results of the measurements with the infrared camera can be seen in figure 13. The temperature maps in figure 13, as well as the simulation results in figure 12, both corresponding to a heat load of $2.5\,\mathrm{W}$ or a flux of $30.8\,\mathrm{mW\,cm^{-2}}$, show that the micro-channel structure has a tendency to cool the left side (outlet) more than the right (inlet). To visualize the temperature distribution across the wafer, the temperature measured at four lines connecting measurement-points are plotted at different flow rates (see figure 10).

The two diagonals (line 1 and 2) in figure 14 and 15 are along the fluid direction but are not following one single channel. Line 1 has a maximal temperature difference of $3.02\,^{\circ}\mathrm{C}$ at the maximum flow rate and line 2 with a maximal temperature difference of $1.66\,^{\circ}\mathrm{C}$. The two diagonals contain points affected by different layout properties. One contains both inlet and outlet whereas the other one contains the Pt100 resistors at the outer corners of the layout with less flow.

In figures 16 and 17 the temperature along the lines 3 and 4 - as indicated in figure 10 - are plotted. Instead of possessing similar temperature gradients, on line 3 the maximal difference of $2.4\,^{\circ}\mathrm{C}$ is much higher than the one on line 4 with a difference of $0.7\,^{\circ}\mathrm{C}$. This is due to the effect of the cold fluent entering at Pt100 resistor 1 and heating up on the way to Pt100 resistor 3.
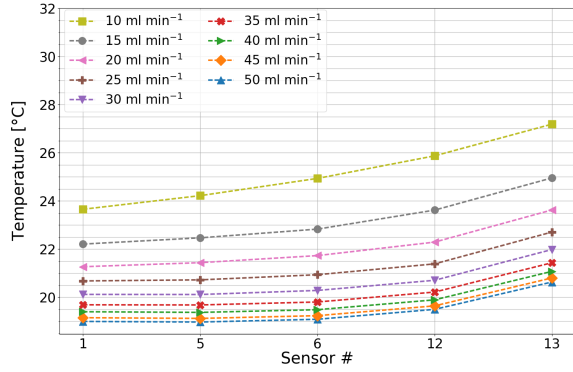
In total the maximum temperature difference across the

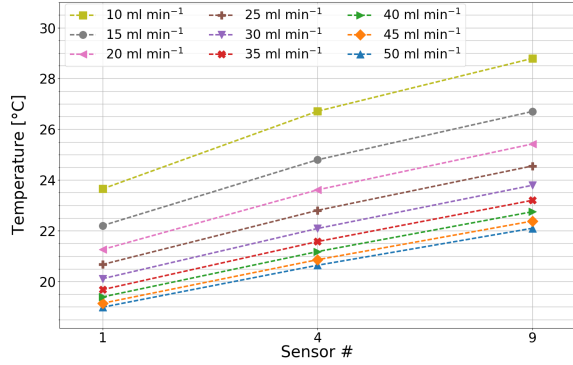Figure 15: Temperature measured along line 2, as indicated in figure 10.

Figure 17: Temperature measured along line 4, as indicated in figure 10.

Figure 16: Temperature measured along line 3, as indicated in figure 10.
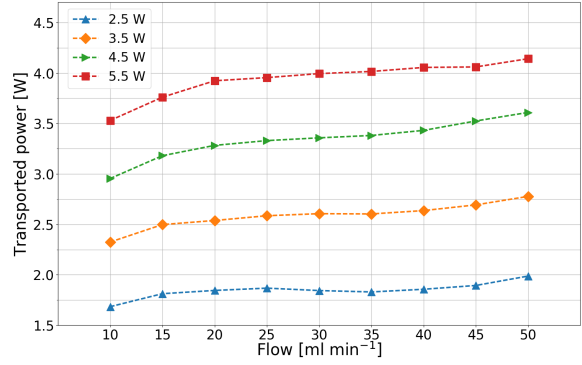
Figure 18: Heat transported by the coolant for different flow rates and heater settings.

wafer surface is 3.4 °C at a flow rate of 50 ml min⁻¹ and a heat load of 30.8 mW cm⁻².

As the difference between the inlet and the outlet temperature directly reflects the heat q_r transported out of the system, the measurement of the temperature at the inlet and the outlet and the coolant specifications can be used to obtain

$$q_r = \dot{m} C_p \Delta T, \qquad (7)$$

with $\dot{m}$ the mass flow, C_p the specific heat capacity and ΔT the temperature difference of the coolant between inlet and outlet. Figure 18 shows the heat removed by the coolant for different flow rates. As can be seen, the values differ from the heater settings by at least 20%. The difference between q_r and the preset heater power represents the losses due to free convection and radiation to the surrounding air and conduction to the Pt100 resistors and NanoPort connectors.

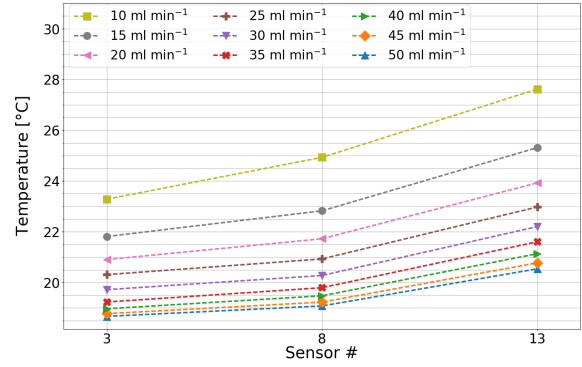The behavior of the effects can also be visualized by a common way to characterize heat sinks, namely by its thermal resistance

$$R = \frac{\overline{T_s} - \overline{T_f}}{q_r}, \qquad (8)$$

which in this case is the difference between the mean fluid temperature $\overline{T_f}$ and the mean surface temperature $\overline{T_s}$ for the transported heat q_r. The mean surface temperature is defined only by the temperatures measured in the middle of the wafer with the Pt100 resistors 5, 6, 7, 10 and 12, to suppress the influence of edge effects - caused by a surplus of not actively cooled material - at the outer border of the channel structure. The thermal resistance, as shown in figure 19, is decreasing with increasing flow rate. A saturation effect is visible for higher flow rates. The difference between the thermal resistance for different heat loads is increasing with higher flow rates, which is caused by the low thermal conductivity of the Pyrex causing a large uncertainty in the measurement of the thermal resistance.
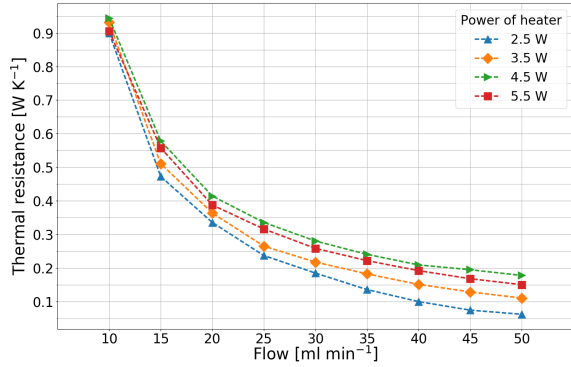
Figure 19: Measured thermal resistance as a function of flow rate. The divergence of the measured values towards higher flow rates is caused by the low thermal conductivity of the Pyrex.
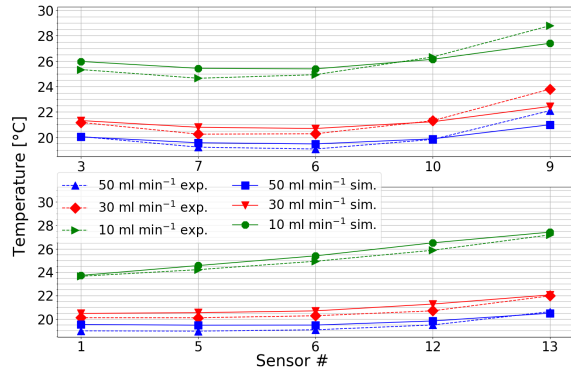

Figure 20: The temperature of the Pt100 resistors on the lines 1 and 2 in the simulation and in the experiment compared with each other for a heat load of $30.8\,\mathrm{mW\,cm^{-2}}$.

5.3. Comparison with simulation

The temperature distribution along the wafer can already be compared through the results from the simulation in figure 12 with the infrared images in figure 13. There is a good agreement between simulation and experimental results, although some slight differences are visible in the areas around the outlet. A more detailed comparison of individual points on the wafer can be seen in figure 20. The inlet temperature was fixed in the simulation and was slightly varying in the experiment due to environmental influences. This discrepancy has been taken into account in figure 20. The measurements were also affected by small variations of the ambient temperature. However, the influence of the ambient air was not implemented in the simulation.

6. Conclusion

A micro-channel structure was designed and produced by DRIE and anodic bonding. The pressure at

the inlet reached a maximum of around 15 bar at flow rates around $50\,\mathrm{ml\,min^{-1}}$, which does not put the device at risk of breaking. Volumetric flows varying from few $\mathrm{ml\,min^{-1}}$ to $50\,\mathrm{ml\,min^{-1}}$ were tested and found to be able to remove enough heat from the micro-channel device to keep the maximum temperature difference over the micro-channel structure below $4\,^\circ\mathrm{C}$ for a heat load of $30.8\,\mathrm{mW\,cm^{-2}}$.

Simulations were set up and tuned with the results of the experiment leading to similar results. An additional tuning of the simulation could be carried out using the values of the actual heat removed by the fluid in the experiment shown in figure 18 to have an accurate model of the heat transfer to the environment within the simulation. Further studies have to address the effect of the remaining material surrounding the micro-channel structure on the thermal measurements and deviations between measurements and the simulations.

Flow and thermal tests show its general feasibility as a large area cooling device. This study demonstrates the first steps of a generic approach of developing a micro-channel structure from silicon. A manifold shape was developed, providing a homogeneous flow across a large channel array, with the potential of being adopted to other sizes, which has not yet been addressed by other HEP experiments cited in this work.

7. Acknowledgment

[1] D. Tuckerman, R. Pease, High-performance heat sinking for VLSI, IEEE Electron Device Letters 2 (1981) 126–129.
[2] A. Sakanova, C. C. Keian, J. Zhao, Performance improvements of microchannel heat sink using wavy channel and nanofluids, International Journal of Heat and Mass Transfer 89 (2015) 59–74.
[3] D. Attree, B. Anderson, E. C. Anderssen, V. Akhnazarov, R. L. Bates, The evaporative cooling system for the ATLAS inner detector, Journal of Instrumentation 07003 (2008) 1–36.
[4] 3M HFE 7100, http://www.3m.com, 2016.
[5] A. Francescon, G. Romagnoli, A. Mapelli, P. Petagna, C. Gargiulo, L. Musa, J. R. Thome, D. Del Col, Development of interconnected silicon micro-evaporators for the on-detector electronics cooling of the future ITS detector in the ALICE experiment at LHC, Applied Thermal Engineering 93 (2015) 1367–1376.
[6] G. Romagnoli, D. A. Feito, B. Brunel, A. Catinaccio, J. Degrange, A. Mapelli, M. Morel, J. Noel, P. Petagna, Silicon micro-fluidic cooling for NA62 GTK pixel detectors, Microelectronic Engineering 145 (2015) 133–137.

[7] A. Nomerotski, J. Buytart, P. Collins, R. Dumps, E. Greening, M. John, A. Mapelli, A. Leflat, Y. Li, G. Romagnoli, B. Verlaat, Evaporative CO_2 cooling using microchannels etched in silicon for the future LHCb vertex detector Module prototype with microchannel cooling, Journal of Instrumentation (2013) 1–12.

[8] B. R. Munson, D. F. Young, T. H. Okiishi, Fundamentals of fluid mechanics, volume 16, Wiley, 4th edition, 2001.

[9] F. Laermer, A. Schilp, Method of anisotropically etching silicon, 1996. US Patent 5,501,893.

[10] A. A. Ayon, R. Braff, C. C. Lin, H. Sawin, M. A. Schmidt, Characterization of a time multiplexed inductively coupled plasma etcher, J. Electrochem. Soc. (1999) pp 339.

[11] M. J. Madou, Fundamentals of microfabrication: the science of miniaturization, CRC Press, 2002. 2nd edition.

[12] K. M. Knowles, A. T. J. Van Helvoort, Anodic bonding, International Materials Reviews (2006) pp. 273–311.

[13] OpenFoam, open source CFD software, http://www.openfoam.com/, 2016.

[14] ANSYS, engineering simulation, http://www.ansys.com/, 2016.

[15] H. M. Wyss, D. L. Blair, J. F. Morris, H. A. Stone, D. A. Weitz, Mechanism for clogging of microchannels, Physical Review E - Statistical, Nonlinear, and Soft Matter Physics 74 (2006) 061402.

[16] ECOM Iota 300 HPLC pump, http://www.ecomsro.com/FS/0001-Ecom/files/products/Info-Iota50-100-300-pump-en.pdf, 2016.

[17] Huber Petite Fleur w, http://www.huber-online.com, 2016.

[18] Bronkhorst miniCori Flow, http://www.bronkhorst.ch, 2016.

[19] Swagelok pressure transducer, http://www.swagelok.com, 2016.

[20] Swagelok valve SS-ORS2, http://www.swagelok.com, 2016.

[21] Swagelok filter SS-2TF-15, http://www.swagelok.com, 2016.

[22] NanoPort Assemblies, https://www.idex-hs.com, 2016.

[23] rs-pro 4inch heater, http://www.rs-online.com, 2016.

[24] infrared VarioCAM HD, http://www.infratec.de, 2016.