Abstract

Porting applications to new hardware or programming models is a tedious and error prone process. Every help that eases these burdens is saving developer time that can then be invested into the advancement of the application itself instead of preserving the status-quo on a new platform.

The Alpaka library defines and implements an abstract hierarchical redundant parallelism model. The model exploits parallelism and memory hierarchies on a node at all levels available in current hardware. By doing so, it allows to achieve platform and performance portability across various types of accelerators by ignoring specific unsupported levels and utilizing only the ones supported on a specific accelerator. All hardware types (multi- and many-core CPUs, GPUs and other accelerators) are supported for and can be programmed in the same way. The Alpaka C++ template interface allows for straightforward extension of the library to support other accelerators and specialization of its internals for optimization.

Running Alpaka applications on a new (and supported) platform requires the change of only one source code line instead of a lot of #ifdefs.

Keywords. Heterogeneous computing, HPC, C++, CUDA, OpenMP, platform portability, performance portability

1 Introduction

1.1 Motivation

Performance gain by employing parallelism in software nowadays faces a variety of obstacles. Parallel performance currently relies on the efficient use of many-core architectures that are commonly found in a heterogeneous environment of multi-core CPU and many-core accelerator hardware.

Heterogeneous systems often expose a memory hierarchy that has to be used efficiently as high computational performance usually requires high memory throughput, demanding the development of efficient caching strategies by application developers.

The same developers face a variety of parallel computing models either specific to a certain hardware or with limited control over optimization. Many models aim for providing easy to learn interfaces that hide the complexities of memory management and parallel execution while promising performance portability, but ultimately fall short of at least one of their aims.

Due to the Herculean effort associated with main-
taining a multi-source application even large development teams thus usually have to choose a strategy of trading performance for portability or vice versa by choosing one single programming model.

Alpaka was designed to prevent this trade off by providing a single source abstract interface that exposes all levels of parallelism existent on today’s heterogeneous systems. Alpaka heavily relies on existing parallelism models, but encapsulates them via a redundant mapping of its abstract parallelization hierarchy [4] to a specific hardware, allowing for mixing various models in a single source C++ code at runtime. Thus, hardware-specific optimizations are possible without the necessity for code replication.

Alpaka therefore is open to future performance optimizations while providing portable code. This is only possible as Alpaka relies on the developers ability to write parallel code by explicitly exposing all information useful for defining parallel execution in a heterogeneous environment rather than hiding the complexities of parallel programming.

Moreover, Alpaka limits itself to a simple, pointer based memory model that requires explicit deep copies between memory levels. This puts the developer in the position to develop portable parallel caching strategies without imposing restrictions on the memory layout. Thus, developers achieve performance portability by skillful code design for which Alpaka provides a single source, explicit redundant parallelism model without any intrinsic optimization hidden from the user.

In the following, we define some categories in order to compare Alpaka to existing models for parallel programming.

**Openness** By Openness we refer to models licensed as open source or defined by an open standard.

**Single source** A model that provides for single source code allows for the application code to be written in a single programming language. It furthermore does not require extensive multiple compilation branches with varying implementations of an algorithm specific to a certain hardware. Single source models may provide annotations (e.g. compiler directives) or add defined words to the language that describe parallel execution.

**Sustainability** We define a sustainable parallel programming model as a model where the porting of an algorithm to another hardware requires minimum changes to the algorithmic description itself. Sustainable models furthermore should be adaptable to future hardware and be available for at least two varieties of current hardware architectures.

**Heterogeneity** Parallel programming models map to heterogeneous systems if they allow for developing a single source code in such a way that execution on various hardware architectures requires minimum specific changes (e.g. offloading, memory scope), execution of a single algorithmic implementation on various architectures can happen in the same program and at the same time during run time.

**Maintainability** We define a parallel programming model to serve code maintainability if it provides a single source code that is sustainable and allows for execution on heterogeneous hardware by changing or extending the programming model rather than the application source code.

**Testability** A model provides testability if an algorithmic implementation can be tested on a specific hardware and give, in a lose sense, the same results when migrating to another hardware. Testability requires sustainability, heterogeneity and maintainability but furthermore demands a separation of the algorithmic description from hardware specific features.

**Optimizability** We define an optimizable model by the fact that it provides the user with complete control over the parallelization of the algorithm as well as the memory hierarchy in a heterogeneous system. Furthermore, fine-tuning algorithmic performance to a specific hardware should not force developers to write multiple implementations of the same algorithm, but rather be provided for by the model.

**Data structure agnostic** A data structure agnostic model does not restrict the memory layout, it instead provides full control over the memory allocation and layout on all hierarchy levels, exposes deep copies between levels and does not assume a certain distribution of the memory over the various hierarchy levels. Specifically, it does not provide distributed data types that are intertwined with the parallelization scheme itself.

**Performance Portability** A model provides per-
formance portability if for a given single source sustainable and maintainable implementation of an algorithm the hardware utilization on various systems is the same within reasonable margins, taking into account the limitations of the specific hardware. Performance portability does not require optimum utilization of the hardware.

2 Related Work

In the following we briefly discuss other libraries targeting the portable parallel task execution within nodes. Some of them require language extensions, others advertise performance portability across a multitude of devices. However, none of these libraries can provide full control over the possibly diverse underlying hardware while being only minimally invasive. Furthermore, many of the libraries do not satisfy the requirement for full single-source (C++) support.

CUDA[3] is a parallel computing platform and programming model developed by NVIDIA. The user is bound to the usage of NVIDIA GPUs. CUDA is not open source and does not provide for Sustainability, heterogeneity, maintainability and testability. For CUDA enabled hardware it provides for optimizability.

PGI CUDA-X86\(^1\) is a compiler technology that allows to generate x86-64 binary code from CUDA C/C++ applications using the CUDA runtime API but does not support the CUDA driver API. Compared to CUDA it allows for heterogeneity, maintainability and testability, but it currently falls behind in adapting to the latest CUDA features, thus has limited support for sustainability. As it does not provide for control of optimizations for X86 architectures, it lacks optimizability.

GPU Ocelot[2] is an open source dynamic JIT compilation framework based onllvm which allows to execute native CUDA binaries by dynamically translating the NVIDIA PTX virtual instruction set architecture to other instruction sets. It supports NVIDIA and AMD GPUs as well as multicore CPUs via a PTX to LLVM translator. The project is not in active development anymore and only supports PTX up to version 3.1 while the current version is 4.2. Thus, it is in many respects similar to PGI CUDA-X86.

**OpenMP**\(^2\) is an open specification for vendor agnostic shared memory parallelization which allows to easily parallelize existing sequential C/C++/Fortran code in an incremental manner by adding annotations (pragmas in C/C++) to loops or regions. Up to version 4.5 there is no way to allocate device memory that is persistent between kernel calls in different methods because it is not possible to create a device data region spanning both functions in the general case. Currently OpenMP does not allow for controlling the hierarchical memory as its main assumption is a shared memory pool for all threads. Therefore, the block shared memory on CUDA devices cannot be explicitly utilized and both heterogeneity and optimizability are not provided for.

**OpenACC**\(^3\) is an open pragma based programming standard for heterogeneous computing which is very similar to OpenMP and provides annotations for parallel execution and data movement as well as run-time functions for accelerator and device management. It allows for limited access to CUDA block shared memory but does not support dynamic allocation of memory in kernel code. It thus does not provide for optimizability and in a practical sense, due to the very limited number of implementations, heterogeneity and sustainability.

**OpenCL**\(^4\) is an open programming framework for heterogeneous platforms. It supports heterogeneity as it can utilize CPUs and GPUs of nearly all vendors. Versions prior to 2.1 (released in March 2015) did only support a C-like kernel language. Version 2.1 introduced a subset of C++14, but there are still no compilers available. OpenCL thus does not support single source programming. Furthermore, it does not allow for dynamic allocation of memory in kernel code and thus does not fully support optimizability.

**SYCL**\(^5\) is an open cross-platform abstraction layer based on OpenCL and thus shares most deficiencies

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1\(\text{https://www.pgroup.com/resources/cuda-x86.htm}\)
2\(\text{http://openmp.org/}\)
3\(\text{http://www.openacc-standard.org/}\)
4\(\text{https://www.khronos.org/opencl/}\)
5\(\text{https://www.khronos.org/sycl/}\)
with OpenCL, however it in principle would allow for optimizability. In contrast to OpenCL it allows for single source heterogeneous programs, but as of now there is no usable free compiler implementation available that has good support for multiple accelerator devices, thus it currently lacks sustainability.

C++ AMP\(^6\) is an open specification from Microsoft which is implemented on top of DirectX 11 and thus currently limited in terms of heterogeneity, sustainability and testability. It is a language extension requiring compiler support that allows to annotate C++ code that then can be run on multiple accelerators. It lacks full control of parallel execution and memory hierarchy and thus falls short of supporting optimizability. Due to restrictions on data types that provide for portability (see e.g. `concurrency::array`) it is not data structure agnostic.

KOKKOS\(^7\) is an open source abstract interface for portable, high-performance shared memory programming and in many ways similar to Alpaka. However, kernel arguments have to be stored in members of the function object coupling algorithm and data together. It thus is not data structure agnostic and in this sense limited in its optimizability.

Thrust\(^1\) is an open source parallel algorithms library resembling the C++ Standard Template Library (STL) which is available for CUDA, Thread Building Blocks\(^8\) and OpenMP back-ends at make-time. Its container objects are tightly coupled with the parallelization strategy, therefore Thrust is not data structure agnostic. Thrust aims at hiding the memory hierarchy and is limited in expressing parallel execution, thus it cannot achieve full optimizability.

Table 1 provides a summary of all related work and a comparison to Alpaka.

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\(^7\)https://github.com/kokkos
\(^8\)https://www.threadingbuildingblocks.org/

3 Introduction to Alpaka

This section serves as an introduction to Alpaka. It first explains the conceptual ideas behind Alpaka, then provides an overview of the hardware abstraction model of Alpaka as well as how the model is mapped to real devices. Lastly, the Alpaka programming API is described.

3.1 Conceptual Overview

Alpaka provides a single abstract C++ interface to describe parallel execution across multiple levels of the parallelization hierarchy on a single compute node. Each level of the Alpaka parallelization hierarchy is unrestricted in its dimensionality. In addition, Alpaka uses the offloading model, which separates the host from the accelerator device.

In order to execute Alpaka code on different hardware the interface is currently implemented using various parallelism models such as OpenMP, CUDA, C++ threads and boost fibers. Alpaka interface implementations, called back-ends, are not limited to these choices and will in the future be extended by e.g. Thread Building Blocks. By design, new back-ends can be added to Alpaka. Thus, Alpaka allows for mixing parallelization models in a single source program, thereby enabling the user to choose the implementation that is best suited for a given choice of hardware and algorithm. It even enables running multiple of the same or different back-end instances simultaneously, e.g. to utilize all cores on a device as well as all accelerators concurrently.

The Alpaka library is based on the C++11 standard without any language extensions and makes extensive usage of C++ template meta-programming. Algorithms are written in-line with single source code and are called kernels which can be compiled to multiple platform back-ends by simply selecting the appropriate back-end. The actual back-ends that execute an algorithm can, thus, be selected at configure-, compile- or run-time, making it possible to run an algorithm on multiple back-ends in one binary at the same time.

Alpaka does not automatically optimize data accesses or data transfers between devices. Data are
Table 1: Properties of intra-node parallelization frameworks and their ability to solve the problems in porting high-performance HPC codes. ✓: yes / fully solved, ○: partially solved, ✗: no / not solved

<table>
<thead>
<tr>
<th>Model</th>
<th>Openness</th>
<th>Single Source</th>
<th>Sustainability</th>
<th>Heterogeneity</th>
<th>Maintainability</th>
<th>Testability</th>
<th>Optimizability</th>
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</table>

stored in simple buffers with support for copies between devices and access to memory is completely data structure agnostic. Thus, the user needs to take care of distribution of data between devices.

Alpaka does neither automatically decompose the algorithmic execution domain and data domain, nor does it assume any default or implicit states such as default device, current device, default stream, implicit built-in variables and functions.

### 3.2 Model of Parallel Abstraction

Alpaka abstracts data parallelism following the redundant hierarchical parallelism model [4], thereby enabling the developer to explicitly take the hierarchy of processing units, their data parallel features and corresponding memory regions into account. The Alpaka abstraction of parallelization is influenced by and based on the groundbreaking CUDA and OpenCL abstractions of a multidimensional grid of threads with additional hierarchy levels in between. Furthermore, it is amended with additional vectorization capabilities.

The four main hierarchies introduced by Alpaka are called grid, block, thread and element level, shown in Figure 1 together with their respective parallelization and synchronization features as discussed below.

Each parallelization level corresponds to a particular memory level (Figure 2): global memory (grid), shared memory (block) and register memory (thread).

The Alpaka model enables to separate the parallelization strategy from the algorithm. The algorithm is described by kernel functions that are executed by threads. A kernel is the common set of instructions executed by all threads on a grid.

The parallelization strategy is described by the accelerator and the work division (See Section 3.3 and 3.4). An accelerator defines the acceleration strategy by a mapping of the parallelization levels

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9Both, CUDA and OpenCL are industry standards for accelerator programming.
Figure 2: The memory hierarchy of the Alpaka abstraction model. Threads have exclusive access to fast register memory. All threads in a block can access the same shared memory. All blocks in a grid can access the same global memory.

to the hardware. The device is the actual hardware onto which these levels are mapped.

3.2.1 Grid

A grid is an n-dimensional set of blocks with a usually large global memory accessible by all threads in all blocks. Grids are independent of each other and can thus be executed either sequentially or in parallel. Grids can be synchronized to each other via explicit synchronization evoked in the code.

3.2.2 Block

A block is an n-dimensional set of threads with a high bandwidth, low latency but small amount of shared memory. All blocks on a grid are independent of each other and can thus be executed either sequentially or in parallel. Blocks cannot be synchronized to each other. The shared memory can only be accessed explicitly by threads within the same block and gets discarded after the complete block has finished its calculation.

3.2.3 Thread

A thread represents the execution of a sequence of instructions. All threads in a block are independent of each other and can thus be executed either sequentially or in parallel. Threads can be synchronized to each other via explicit synchronization evoked in the code. Threads can by default always access their private registers, the shared memory of the block and the global memory\textsuperscript{10}. All variables within the default scope of a kernel are stored within register memory and are not shared between threads. Shared and global memory can be allocated statically or at runtime before the kernel start.

3.2.4 Element

The element level represents an n-dimensional set of elements and unifies the data parallel capabilities of modern hardware architectures e.g. vectorization on thread level. This is necessary as current compilers do not support automatic vectorization of basic, non-trivial loops containing control flow statements (e.g. if, else, for) or non-trivial memory operations. Furthermore, vectorization intrinsics as they are available in intrin.h, arm_neo.h, altivec.h are not portable across varying back-ends. Alpaka therefore currently relies on compiler recognition of vectorizable code parts. Code is refactored in such a way that it includes primitive inner loops over a fixed number of elements.

The user is free to sequentially loop over the elements or to utilize vectorization where a single instruction is applied to multiple data elements in parallel e.g. by utilizing SIMD vector registers. Processing multiple elements per thread on some architectures may enhance caching.

3.3 Mapping of Abstraction to Hardware

Alpaka clearly separates its parallelization abstraction from the specific hardware capabilities by an explicit mapping of the parallelization levels to the hardware. A major point of the hierarchical parallelism abstraction is to ignore specific unsupported levels of the model and utilize only the ones sup-

\textsuperscript{10} However, Alpaka allows for atomic operations that serialize thread access to global memory.
ported on a particular device. Mapping is left to the implementation of the accelerator.

This allows for variable mappings as shown in the examples below and, therefore, an optimum usage of the underlying compute and memory capabilities—albeit with two minor limitations: The grid level is always mapped to the whole device being in consideration and the kernel scheduler can always execute multiple kernel grids from multiple streams in parallel by statically or dynamically subdividing the available resources.

Figure 3 shows a mapping of the Alpaka abstraction model onto a CPU, a many integrated cores device (MIC) and a GPU architecture. For the MIC architecture a second mapping is shown, which spans a block over all cores to increase the shared memory. CPU and MIC process multiple elements per thread and benefit from their vectorization units, while a GPU thread processes only a small amount of elements.

![Mapping Diagram](image)

Figure 3: Possible mapping of blocks, threads and elements to a MIC, a CPU and a GPU device. The mapping can skip individual levels when they are not beneficial on a particular device.

Finally, the user needs to decide which back-end to use for which device. It can be selected from the set of predefined accelerators or the user can write its own accelerator implementation. The set of predefined accelerator mappings are listed in Table 2.

<table>
<thead>
<tr>
<th>Arch</th>
<th>Acc</th>
<th>Grid</th>
<th>Block</th>
<th>Thread</th>
<th>Element</th>
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<td>( N )</td>
<td>( B \cdot V )</td>
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<td>CPU</td>
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<td>( N )</td>
<td>( V )</td>
<td>1</td>
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<tr>
<td></td>
<td>OpenMP thread</td>
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<td>( B \cdot V )</td>
<td>1</td>
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<td>C++11 thread</td>
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<td>( V )</td>
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<td>( V )</td>
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<td>OpenMP thread</td>
<td>1</td>
<td>( N )</td>
<td>( B \cdot V )</td>
<td>1</td>
</tr>
</tbody>
</table>

### 3.4 Alpaka Programming Interface

In the following each part of the Alpaka interface is described briefly. The provided listings assume that the Alpaka namespace is used. Source code examples are provided to give a more detailed insight into Alpaka.

#### 3.4.1 Kernel

The kernel is the central unit in Alpaka that acts as the bridge between host and accelerator code through a C++ class or a C++ lambda (C++14 required). The algorithm is described from the block down to the element level which removes the need for a nested loop structure like it is used in OpenMP and SYCL. The kernel function object needs to implement the template `operator()` member function as it is shown in Listing 1. This member function is the first function called on the particular accelerator device.

The code within the kernel is written in C++11 (restricted by the utilized back-end compilers) with additional calls to the Alpaka run-time API. There exist no implicit built-in variables and functions like it is usual in CUDA or OpenCL. All information can be retrieved from the accelerator object (Listing 1 : 4).
struct Kernel {
    template <class T_Acc, class T>
    ALPAKA_FN_ACC void operator()(T_Acc acc, T data) const {
        /* Write kernel code here */
    }
};

Listing 1: A skeleton of an Alpaka kernel. The kernel needs to implement the operator() with prefix ALPAKA_FN_ACC, which takes at least the accelerator as parameter.

Vec<Dim2, size_t> elementsPerThread(1,1);
Vec<Dim2, size_t> threadsPerBlock(1,1);
Vec<Dim2, size_t> blocksPerGrid(8,16);
workdiv::WorkDivMembers<Dim2, size_t>
    (blocksPerGrid, threadsPerBlock, elementsPerThread);

Listing 2: Declaration of a work division in the host code. The work division is defined in two dimensions for all levels. Element and block level have an extent of one, while the grid has an extent of 128.

3.4.2 Accelerator Executable Functions

Alpaka defines the macros ALPAKA_FN_HOST, ALPAKA_FN_ACC and ALPAKA_FN_HOST_ACC to define that functions are callable from host, from accelerator or from both host and accelerator device. All functions called from accelerator code need to be prefixed by these macros.

3.4.3 Work Division and Index Retrieval

The work division defines the extent and dimensionality of each level of the Alpaka abstraction model. Listing 2 shows the declaration of a two-dimensional work division on the host where the grid level has an extent of 128 blocks and the other levels have an extent of one.

ALPAKA_FN_ACC void operator()(T_Acc acc) const {
    // Retrieve the global n-dim thread index
    auto gTIdx = idx::getIdx<Grid, Threads>(acc);
    // Retrieve the n-dim thread extent
    auto gTExtent = workdiv::getWorkDiv<Grid, Threads>(acc);
    // Retrieve the global one dim thread index
    auto linIdx = core::mapIdx<1>(gTIdx, gTExtent);
}

Listing 3: Access of work division and thread index. Thread extent and index are mapped onto a one dimensional space to retrieve a linearized index.

The work division declared in Listing 2 can be accessed within the kernel via the accelerator object. Furthermore, there exist methods to map the index space between varying extents and dimensionalities. Listing 3 shows a kernel function that calculates the global linearized index of a thread with the help of Alpaka run-time functions.

3.4.4 Memory

Alpaka provides simple memory buffers that store the plain pointer to memory of the particular device and additional information like residing device, extent, pitch and dimension. These buffers are uniform for all devices which allows for copying memory between different devices with respect to pitch and extents, see Listing 4.

3.4.5 Streams

A stream is the work queue of a particular device. Operations in streams are always executed in-order: No operation in a stream will begin before all previously issued operations in the stream have completed. Streams can be synchronous or asynchronous with respect to operations on the host. If an operation is
// Dim, data and index type
using Dim = dim::DimInt<2>;
using Data = std::uint32_t;
using Size = std::size_t;

// Declare extents of buffer
Vec<Dim, Size> extents(10, 10);

// Declare host and device buffer
auto hostBuf = mem::buf::alloc<Data, Size>(host, extents);
auto devBuf = mem::buf::alloc<Data, Size>(dev, extents);

// Copy host buffer to device buffer
mem::view::copy(stream, devBuf, hostBuf, extents);

Listing 4: Allocation of a two dimensional host and a device buffer with one hundred elements each. Moreover, the host buffer is copied to the device buffer.

Listing 5: Full example of a kernel execution. The kernel is executed with a work division of 256 blocks and 16 threads per block on a single accelerator (in this case the sequential CPU back-end is selected).

3.4.6 Kernel Execution

A kernel will be executed by enqueuing a kernel executor into a stream of a particular device. An executor binds an accelerator, a work division, a kernel and its parameters. Streams are filled with those executors and Alpaka takes care that they will be executed in the specified way. Listing 5 shows a full host code example from the accelerator type definition up to the enqueuing of a kernel into a stream.

4 Evaluation

This section provides an evaluation of Alpaka on a variety of hardware platforms using various back-ends, see Table 3. All CUDA evaluations are compiled with CUDA 7.0 and all CPU evaluations with gcc 4.9.2. Source codes denoted as native are not wrapped by Alpaka, but contain pure CUDA or OpenMP code.

The evaluation was performed in five stages: First, the PTX and assembler code generated during compilation of an Alpaka DAXPY program is compared to the respective native versions. Then, the overhead of two naive Alpaka DGEMM kernels with respect to their native versions is measured. As a next step, it is investigated what happens to performance portability when the naive Alpaka DGEMM kernels...
are mapped to an inappropriate back-end followed by the description of a single source DGEMM kernel and how it can obtain performance portability with the help of Alpaka. Finally, the applicability of Alpaka to real world applications was evaluated using HASEonGPU [5].

4.1 Conceptual Comparison

This section compares the Alpaka implementation of the generalized vector addition algorithm in double precision (DAXPY) to a sequential C++ and CUDA implementation on the source code and assembler level.

DAXPY computes \( Y \leftarrow \alpha X + Y \) where \( X \) and \( Y \) are vectors while \( \alpha \) is a scalar. DAXPY was selected as a trivial example on the one hand to showcase the non-obfuscation abstraction and on the other hand the zero overhead abstraction of Alpaka. The source code of the various DAXPY implementations are available in our GitHub repository\(^{11}\).

From a developers point of view, the source codes are very similar to each other. However, Alpaka related changes are necessary: Alpaka adds the additional accelerator template argument together with the according function argument to the kernel function call. Each function that should be called from a accelerator needs to be annotated with the Alpaka specific macro `APLAKA_FK_ACC`. Furthermore, Alpaka replaces the for loop index calculations by an Alpaka equivalent that calculates the correct index for each thread.

Figure 4 shows snippets of the PTX code of the compiled Alpaka and CUDA implementations.

Comparing the generated PTX code leads to the result that these codes are identical up to two additional but unused function parameters in the Alpaka variant as well as different internal variable names and the use of non coherent texture cache once. It can be seen that modern compilers are able to remove all the meta-programming abstraction introduced by Alpaka. This perfectly demonstrates the zero overhead abstraction of the Alpaka interface regarding the CUDA interface.

\(^{11}\)https://github.com/BenjaminW3/vecadd

![Figure 4: Snippet of the PTX code of Alpaka and CUDA kernels. The PTX code is the same up to the line where the CUDA PTX uses non coherent texture cache. This cache allows for access with higher bandwidth and lower latency.](image)

The assembler code of the native C++ implementation does not perfectly fit the Alpaka assembler since only the native implementation has been vectorized to use the packed double precision SSE2 instructions `movdp`, `muldp` and `addpdp` instead of the single value versions `movd`, `mulsd` and `addsd`. However, by looping over the additional data level of the Alpaka abstraction model which has a constant size, the compiler recognizes the iteration independent looping pattern and optimizes this by using SIMD instructions to process multiple consecutive iterations together.

4.2 Performance

As a next step, the performance characteristics of the CUDA and OpenMP Alpaka back-ends are evaluated. First, an algorithm is implemented for both Alpaka and the particular native API to show the pure Alpaka overhead in numbers. Then, the native Alpaka kernel is mapped to the non-native back-end to show that Alpaka is not naïve performance portable. Afterwards, an enhanced single source Alpaka kernel is introduced and mapped to various architectures and it is shown that it can match the performance of the native implementations when using the appropriate Alpaka back-ends.

For comparison the double generalized matrix-multiplication (DGEMM) has been selected as a compute bound problem. DGEMM computes
Table 3: List of utilized accelerator hardware for evaluation. Clock frequencies which are encapsulated in braces denote the turbo frequency of the particular architecture. Often turbo can only be utilized when not all cores of a device are busy.

<table>
<thead>
<tr>
<th>Vendor</th>
<th>AMD</th>
<th>Intel</th>
<th>Intel</th>
<th>NVIDIA</th>
<th>NVIDIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>Opteron 6276</td>
<td>Xeon E5-2669</td>
<td>Xeon E5-2630v3</td>
<td>K20 GK110</td>
<td>K80 GK210</td>
</tr>
<tr>
<td>Number of devices</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Number of cores per device</td>
<td>16</td>
<td>4</td>
<td>8 (16 hyper-threads)</td>
<td>2064</td>
<td>2x2406</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>2.3 (3.2) GHz</td>
<td>2.4 GHz</td>
<td>2.4 (3.2) GHz</td>
<td>0.56 (0.88) GHz</td>
<td>2.5 GHz</td>
</tr>
<tr>
<td>Th. double peak performance</td>
<td>480 GFLOPS</td>
<td>160 GFLOPS</td>
<td>540 GFLOPS</td>
<td>1170 GFLOPS</td>
<td>2x1450 GFLOPS</td>
</tr>
</tbody>
</table>

$C \leftarrow \alpha AB + \beta C$ where $C$, $A$ and $B$ are matrices $A = (a_{i,j})$, $B = (b_{i,j})$ while $\alpha$ and $\beta$ are scalars. DGEMM implementations can utilize all levels of parallelism on GPUs and CPUs ranging from blocking over shared memory to vectorization, providing a perfect showcase of these techniques within the Alpaka library. All DGEMM implementations are available in our GitHub repository.

All input matrices are dense and always have square extents to minimize bias towards implementations preferring column- or row-major layout. Initially, the matrices are filled with random values in the range [0.0, 10.0]. The matrices are mapped to 1D memory buffers with Alpaka aligning rows to optimum memory boundaries. Measurements do not include times for allocating the matrices on the host, filling them, a possible data transfer between the processor and a co-processor as well as device and stream initialization.

![Graph showing the speed of the Alpaka kernels mapped to the corresponding native back-ends relative to their native implementations](image)

Figure 5: The native Alpaka kernels were mapped to their corresponding native back-ends and compared to the native implementations. Both kernels show a relative overhead of less than 6% which is well below run-to-run variation. This proves the zero overhead abstraction of Alpaka.

4.2.1 Zero Overhead Abstraction

Alpaka does not add additional overhead to the algorithm execution time. In order to show this zero overhead, native CUDA and OpenMP 2 kernels were translated one-to-one to Alpaka kernels.

The CUDA kernels use a block parallelized tiling algorithm based on the CUDA programming guide ([3], Sec. 3.2.3) and were executed on a compute node with a NVIDIA K20 GK210. The OpenMP kernels use a standard DGEMM algorithm with nested for loops and were executed on a compute node with two Intel E5-2630v3 CPUs. The kernels were executed with an increasing matrix size and their execution time was measured. Figure 5 shows the speed of the Alpaka kernels mapped to the corresponding back-end relative to their native implementations.

The native CUDA Alpaka kernel provides more than 94% relative performance for almost all matrix sizes, which is an overhead of 6% or less. After a deep inspection of the compiled PTX code it turned out that this overhead results from move and forward operators translated to copies. These operators are used for grid index calculations within an Alpaka kernel. Furthermore, a small number of additional CUDA runtime calls by the alpaka CUDA back-end are necessary. The native OpenMP Alpaka kernel provides an average relative performance of 100%.

12https://github.com/BenjaminW3/matsmul
NVIDIA CUDA (nvcc) and the gcc compiler remove all the abstraction layers introduced by Alpaka.

A naïve port of a kernel to an architecture it was not meant to be executed on will almost always lead to poor performance. Thus, providing a single, performance portable kernel is not trivial. The following section shows that Alpaka is able to provide performance for various back-ends with a single source kernel.

4.2.2 Single Source Kernel / Performance

It is possible to write a single source kernel that performs well on all tested Alpaka back-ends without a drop in performance compared to the native implementations. In order to reach this performance, the developer needs to abstract the access to data, optimize the work division, and consider cache hierarchies. The single source Alpaka DGEMM kernel implements a tiling matrix-matrix multiplication algorithm and considers the architecture cache sizes by adapting the number of elements processed per thread or block and the size of the shared memory to provide minimal access latency. A lot of processor architectures benefit from the Alpaka element level parallelism when calculating multiple elements in parallel in the vector processing unit.

Figure 7 provides a brief description of the hierarchical tiling algorithm. A block calculates the result of a tile in matrix C. Each thread in this block loads a set of elements of matrices A and B into shared memory to increase memory reuse. It then calculates the partial results of its set of elements before the block continues with the next tiles of A and B.

Figure 8 shows the performance of the tiling kernel mapped to the CUDA and OpenMP back-ends relative to the original native implementations. No performance loss compared to native implementations is observed but instead performance gain in the majority of cases is seen. This is due to the more descriptive nature of the Alpaka kernel which enables even further optimizations by the back-end compilers.

It is clear that there exist even more optimized versions of the algorithm, e.g. in mathematical libraries such as cuBlas, which is fine tuned for differ-

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13In this case the triple nested loop is compiled using the CUDA back-end, while the tiled shared-memory version is mapped to OpenMP.
Figure 7: An Alpaka optimized hierarchically tiled matrix-matrix multiplication algorithm with multiple elements per thread. A block loads tiles of the A and B matrix into its shared memory to increase memory reuse. A thread can calculate multiple elements by using the vector processing unit of its particular backend.

Figure 8: The Alpaka single source DGEMM kernel implements a hierarchical tiling matrix-matrix multiplication algorithm. This kernel can compete with and even outperform the original native implementations on all tested back-ends.

4.2.3 Performance Portability

Figure 9 shows the performance of the Alpaka tiling kernel executed on varying architectures relative to the theoretical peak performance of the corresponding architecture. The kernel work division was selected in a way that provides good performance for the particular architecture. CPU devices were accelerated by the OpenMP 2 back-end, while NVIDIA devices were accelerated by the CUDA back-end. The performance of all architectures lies around 20% of the theoretical peak performance. This shows that a single Alpaka kernel using all levels of the abstraction model together with optimized data access patterns is able to provide performance portability over various architectures.

4.3 Real World Example

HASEonGPU is an open-source adaptive massively parallel multi-GPU Monte Carlo integration algorithm for computing the amplified spontaneous emission (ASE) flux in laser gain media pumped by pulsed lasers\textsuperscript{14}.

The source code consists of about ten thousand lines of code and has been ported in three weeks by one person to Alpaka (HASEonAlpaka). After the porting has been finished, HASEonAlpaka has successfully been executed on GPU and CPU clusters.

Figure 10 shows the relative speed of a HASEonAlpaka computation executed with identical parameters on different systems. The original native CUDA version is used as the basis for comparison. The Alpaka version using the CUDA back-end running on the same NVIDIA K20 GK110 cluster as the native version does not show any overhead at all leading to identical execution times.

\textsuperscript{14}\url{https://github.com/ComputationalRadiationPhysics/haseongpu}
5 Conclusion

We have presented the abstract C++ interface Alpaka and its implementations for parallel kernel execution across multiple hierarchy levels on a single compute node. We have demonstrated platform and performance portability for all studied use cases. A single source Alpaka DGEMM implementation provides consistently 20% of the theoretical peak performance on AMD, Intel and NVIDIA hardware, being on par with the respective native implementations. Moreover, performance measurements of a real world application translated to Alpaka unanimously demonstrated that Alpaka can be used to write performance portable code.

Performance portability, maintainability, sustainability and testability were reached through the usage of C++ metaprogramming techniques abstracting the variations in the underlying architectures. Alpaka code is sustainable, optimizable and easily extendable to support even more architectures through the use of C++ template specialization. It is data structure agnostic and provides a simple pointer based memory model that requires explicit deep copies between memory levels.

Future work will focus on including more Alpaka back-ends, e.g. for OpenACC and OpenMP 4.x target offloading and studying performance portability for additional architectures (e.g. Intel Xeon Phi and OpenPower) and applications.

Alpaka is an open-source project and available in our GitHub repository\textsuperscript{15}.

References


\textsuperscript{15}https://github.com/ComputationalRadiationPhysics/alpaka
