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MuPix7 – A fast monolithic HV-CMOS pixel chip for Mu3e

H. Augustin,^a N. Berger,^b S. Dittmeier,^a J. Hammerich,^a U. Hartenstein,^b Q. Huang,^b
L. Huth,^a D. Immig,^a A. Kozlinskiy,^b F. Meier Aeschbacher,^{a,1} I. Perić,^c A.-K. Perrevoort,^a
A. Schöning,^a S. Shrestha,^{a,2} I. Sorokin,^b A. Tyukin,^b D. vom Bruch,^b F. Wauters,^b
D. Wiedner,^a M. Zimmermann^b on behalf of the Mu3e collaboration

^aUniversität Heidelberg, Physikalisches Institut, Im Neuenheimer Feld 226, 69120 Heidelberg, Germany

^bInstitut für Kernphysik, Johann-Joachim-Becherweg 45, Johannes Gutenberg-Universität Mainz, 55128 Mainz, Germany

^cInstitut für Prozessdatenverarbeitung und Elektronik, KIT, Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein-Leopoldshafen, Germany

E-mail: meier@physi.uni-heidelberg.de

ABSTRACT: The MuPix7 chip is a monolithic HV-CMOS pixel chip, thinned down to 50 μm . It provides continuous self-triggered, non-shuttered readout at rates up to 30 Mhits/chip of $3 \times 3 \text{ mm}^2$ active area and a pixel size of $103 \times 80 \mu\text{m}^2$. The hit efficiency depends on the chosen working point. Settings with a power consumption of 300 mW/cm^2 allow for a hit efficiency $> 99.5\%$. A time resolution of 14.2 ns (Gaussian sigma) is achieved. Latest results from 2016 test beam campaigns are shown.

KEYWORDS: Particle tracking detectors (Solid-state detectors), Performance of High Energy Physics Detectors

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¹Corresponding author.

²Now at Middle Tennessee State University

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1 Introduction

CMOS pixel detectors are successfully used for tracking detectors in particle physics since years. They provide a cost-effective alternative to hybrid designs, come with small pixel sizes and can be thinned down to $50\text{ }\mu\text{m}$. Their use in high-rate environments was limited by readout deadtime (shuttered readout) and charge collection limits (thin depletion zones, electron diffusion). The MuPix7 is a pixelated silicon detector made with industry-standard high-voltage CMOS technology, based on the principles described in [1]. This allows to apply a bias voltage of up to -85 V , hence electron drift dominates. The chip has an array of 32×40 pixel cells, sized $103 \times 80\text{ }\mu\text{m}^2$ each. The charge-sensitive amplifier and the line driver are on top of the (deep-implant) sensor diode in the pixel matrix. The signal is transmitted via a single-ended transmission line to the mirroring digital pixel in the periphery which contains an amplifier, a tuneable comparator, and a time-stamp generator. This design choice protects the analog part from digital noise by separation and results in a fast, zero-suppressed readout that operates continuously without a trigger. Any rate limit comes from shaping time in the pixel cell and the data readout capabilities. The need for many connections from the active array to the periphery consumes space and imposes limits on the integration density, leading to somewhat larger pixels compared to other monolithic CMOS pixel chips. A more detailed description of the MuPix7 chip can be found elsewhere [2]. This report provides new results to the ones reported therein.

The results shown below have all been obtained in 4-plane telescope setups [3] made with thinned MuPix7 chips, unless where noted differently. Tracks were established from three hits and extrapolated to the device under test (DUT). Unless where stated differently, a matching hit on the DUT has to be within a radius of $800\text{ }\mu\text{m}$ around the extrapolated track center and within a time window of $\pm 48\text{ ns}$ with respect to the track time.

2 Efficiency studies

The MuPix7 chip performance is controlled by a number of voltage settings, steered by internal DACs. These settings can be optimised for a variety of performance targets, which are mainly efficiency and time resolution, both at the expense of noise level and power consumption. The power consumption was measured on the external power lines. The efficiency and noise level as function of threshold was measured at four choices of settings and are shown in Fig. 1. The chip can be operated with an efficiency well above 99.5% at power ratings equal or below 400 mW/cm².

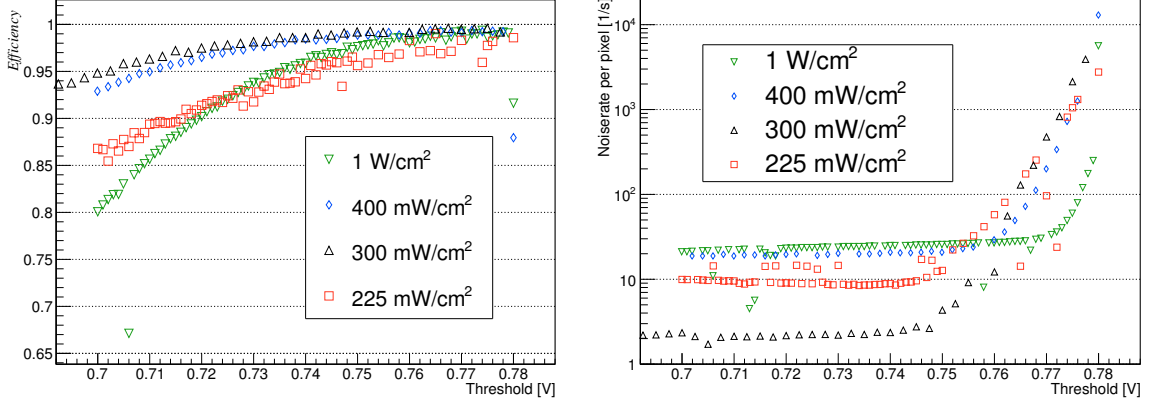


Figure 1. Efficiency (left) and noise (right) as function of threshold for different power settings (higher voltage corresponds to lower comparator threshold). Measured at PSI π M1, mixed π^+ , μ^+ , e^+ beam at 224 MeV momentum setting.

Using the EUDET telescope at DESY [4], we made use of the excellent spatial resolution of the MIMOSA26 chips (about 4 μ m at the chosen configuration, measured using track to hit residuals, perpendicular beam incidence) and studied the efficiency of the MuPix7 with sub-pixel resolution by extrapolating the track from the EUDET planes to the MuPix7 DUT. To enhance effects, the threshold of the MuPix7 was detuned targeting a lower overall efficiency. In the MuPix design, charge sharing between neighbouring pixels is a minor effect on the percent level. This is a consequence of the small depletion zone (about 15 μ m) compared to the pixel cell size and the fast charge collection. Raising the threshold (i.e. lowering the threshold voltage) should therefore lower the efficiency for hits at the edges and corners. The results in Fig. 2 (left) clearly show this effect. This can be compensated by turning the sensor by 45° with respect to the beam axis, which increases the effective length of the depletion zone by $\sqrt{2}$, also shown in Fig. 2 (right).

3 Time resolution

In a previous publication [2] we reported a timing resolution of 11 ns (expressed as Gaussian σ), measured using the settings corresponding to a power consumption of 1000 mW/cm². We repeated that measurement using the same setup, where the telescope was amended with scintillators (time resolution about 1 ns) for obtaining the timing reference. The radius for a matching hit was set to a tight value of 120 μ m and the χ^2 per degree of freedom of the track fit was required to be less than 5. Operating the chip at 300 mW/cm², a timing resolution of 14.2 ns was measured (averaged over all

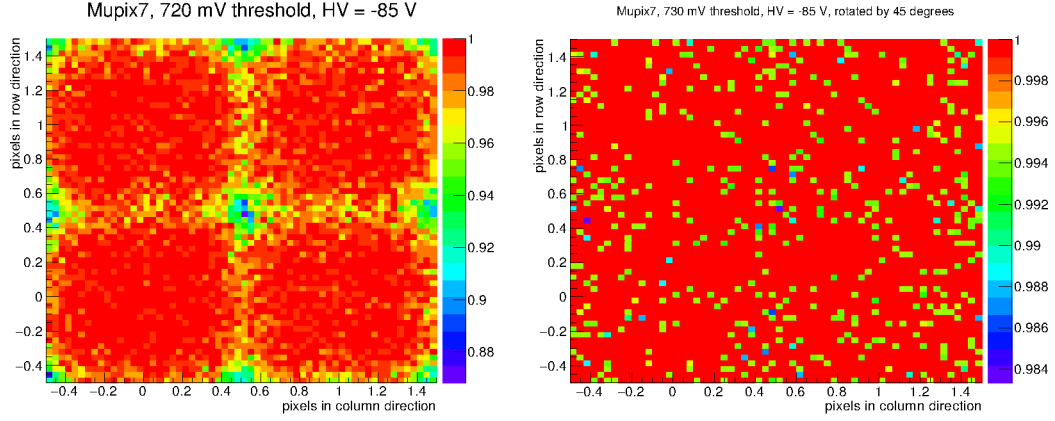


Figure 2. Efficiency map with sub-pixel resolution. Left: Sensor perpendicular to beam axis. Right: Sensor inclined by 45° w.r.t. beam axis. The chip is intentionally operated at higher threshold to force lower overall efficiency for effect enhancement. Hits of all pixels of the chip superimposed on 2×2 pixels to enhance the number of entries per bin. Units are pixel size. Measured at DESY using electrons at 4 GeV.

pixels of the DUT), see Fig. 3. This result meets the Mu3e requirements of a timing resolution better than 20 ns.

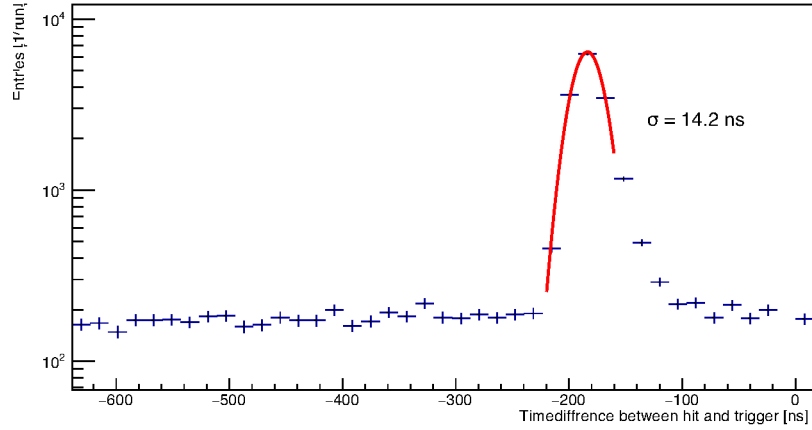


Figure 3. Timing resolution measured using settings with a power consumption of 300 W/cm^2 . Shown is the difference in time between the hit in the DUT and the scintillators. Bin size is 16 ns. Measured at DESY using electrons at 4 GeV.

4 Crosstalk

An extensive search for crosstalk has been carried out. No signs have been found except for a peculiar case tied to the arrangement of the transfer lines. In our telescope setup, events with 3 hits on the DUT have been studied. One of these hits must be compatible with a track fitted through the three reference planes. Such events occurred at a rate of a few percent for a typical choice of threshold where the three hits were spaced by an empty pixel. Within a column, the transfer lines are routed in groups of even and odd row addresses, hence the empty pixel in between the hits. The

spacing of the lines is the same for most of the lines with a few exceptions. The missing entries for certain row addresses, see Fig. 4, nicely match those cases with increased spacing. The crosstalk appears to originate from neighbouring transfer lines along the pixel column. To mitigate the effect, an adjustment to the line driver seems to be sufficient and will be implemented in the next version of the chip.

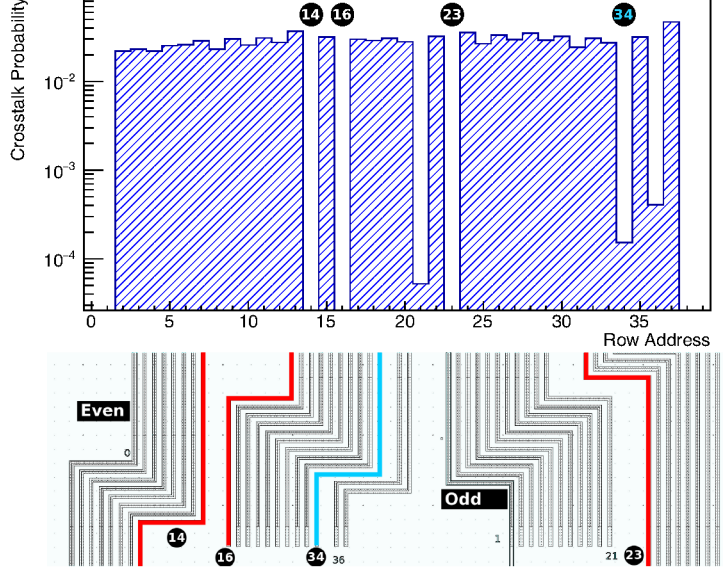


Figure 4. Top: Crosstalk probability. See main text for explanation. Bottom: Layout of transmission lines from analog pixel down to digital pixel cell. Lines in red and blue intentionally emphasised to indicate lines with bigger spacing.

5 High rate performance

Rate dependent effects in the pixel cell have been tested in a high rate setup at MAMI. A beam of electrons at an energy of 855 MeV was focused on a sub-array of 5×5 pixels, keeping the overall hit rate well below any readout limitations. The analysis used a bigger time window of ± 80 ns. No rate dependency on the efficiency of the DUT has been observed for rates up to 2.2×10^6 Hz/ 25 pixels, which corresponds to 1070 MHz/cm², see Fig. 5. This is well above the rate of 2.5 MHz/cm² required for the Mu3e experiment during phase I. For comparison, the serialiser of the chip works at 1.25 Gbits/s. One hit consumes 40 bits (8b10b encoded including comma word), hence one data link is capable of handling at least 30 Mhits/s. Or, a chip featuring the design target area of 20×20 mm² will be limited to 7.8 Mhits / (s · cm²) by one such link.

6 Discussion and outlook

The MuPix7 chip has shown excellent performance, meeting requirements for the upcoming Mu3e experiment. In essence, at settings with a power consumptions of 300 mW/cm², an efficiency of

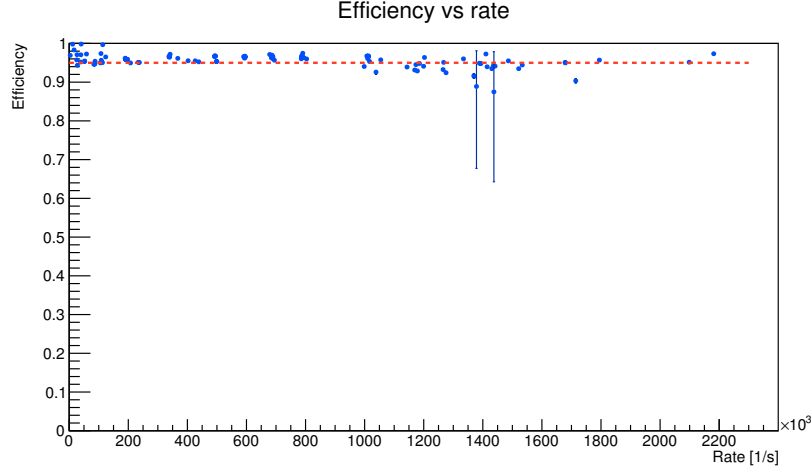


Figure 5. Efficiency of the DUT plane at varying hit rates on a 5×5 pixel array. Horizontal line added at arbitrary value of 0.95 to guide the eye.

better than 99.5% and a time resolution of 14.2 ns have been measured. The sustainable data rate is way above the requirements.

While MuPix7 is a great success, it is still a test chip. The next version, MuPix8, is under way at time of writing. Among the changes are the enlargement of the column size to cover the target length of about 20 mm (for use with Mu3e), mitigation and optimisation of the crosstalk, optimise pad layout for module integration studies, and the number of data links will be increased to 3. The latter will enable the chip to handle up to 94 Mhits/s or about 23 Mhits / (s · cm²).

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