Development of n-in-p pixel modules for the ATLAS upgrade at HL-LHC

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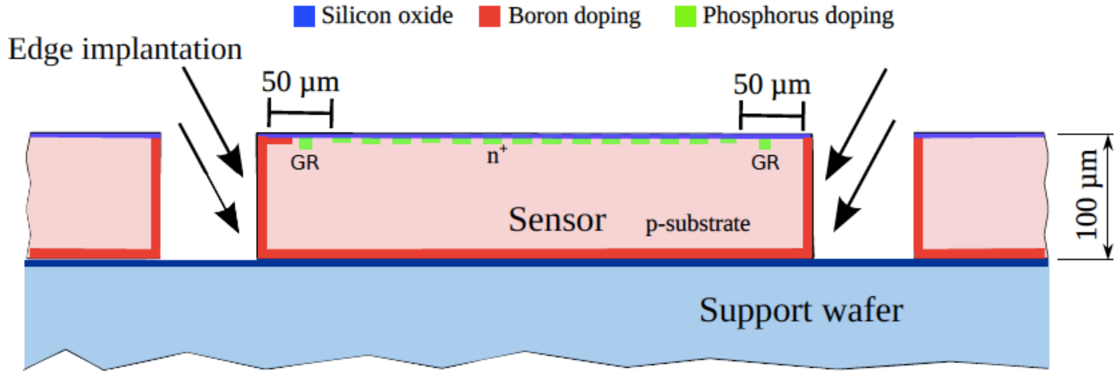
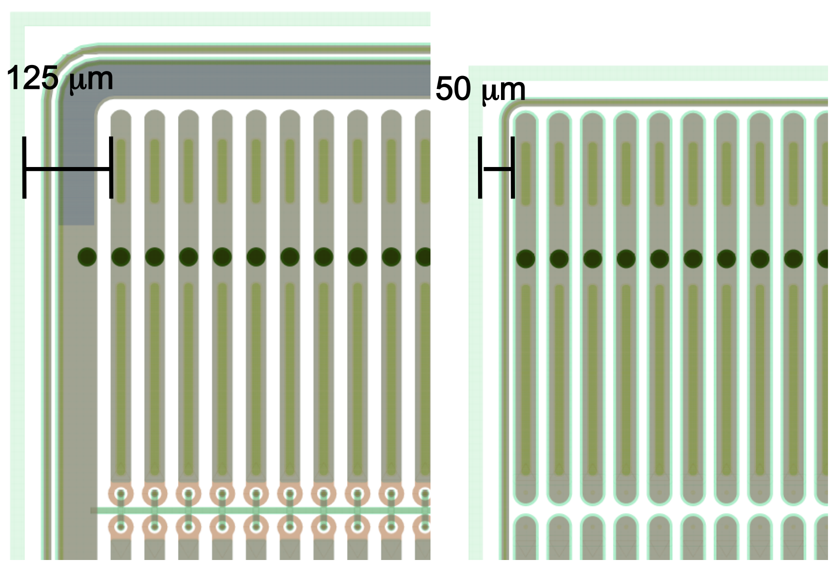
Introduction

- Performance of n-in-p pixel sensors with different thickness:
  - Charge collection
  - Hit efficiency
  - Power dissipation
- Optimization of punch-through structures based on beam-test studies
- New pixel sensors designs for new chips in 65 nm technology of the RD53 Collaboration
- Performance studies for 50 μm x 50 μm pixels at high pseudo-rapidity
- On-going productions of thin n-in-p pixel sensors at ADVACAM and CIS

Thin n-in-p pixel sensor production at VTT



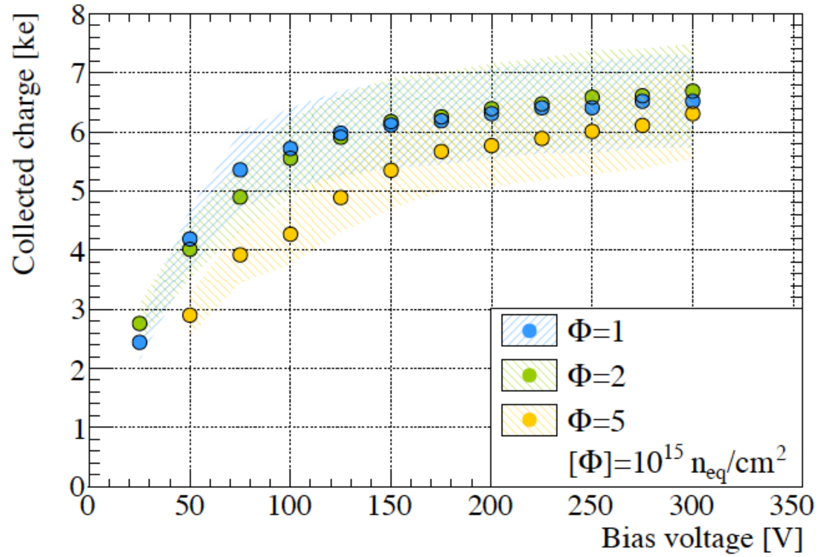
- n-in-p pixels on FZ and MCZ material
- 100 µm and 200 µm thickness
- Flip-chipping performed at VTT after removal of support wafer

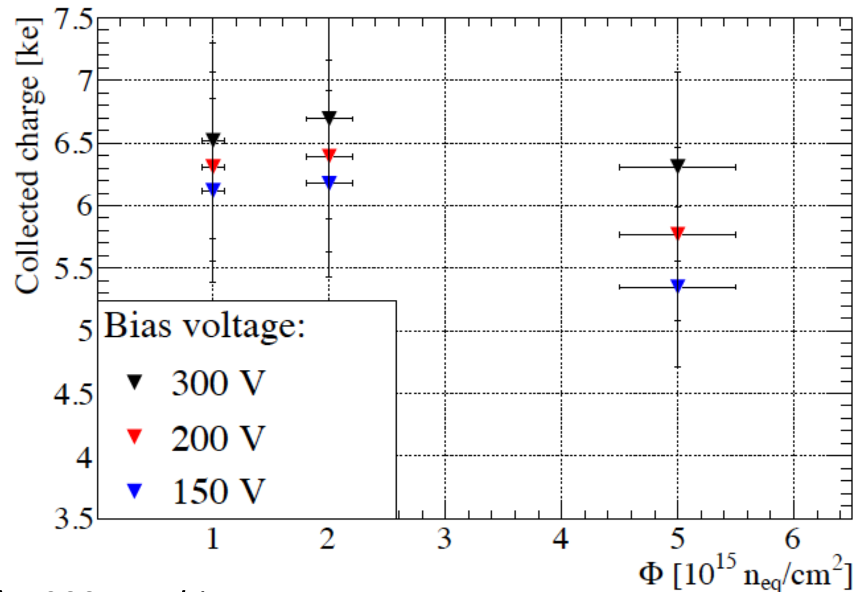


- 125 µm edge implemented In FE-I3 and FE-I4 sensors
- 50 µm implemented only in FE-I3 sensors

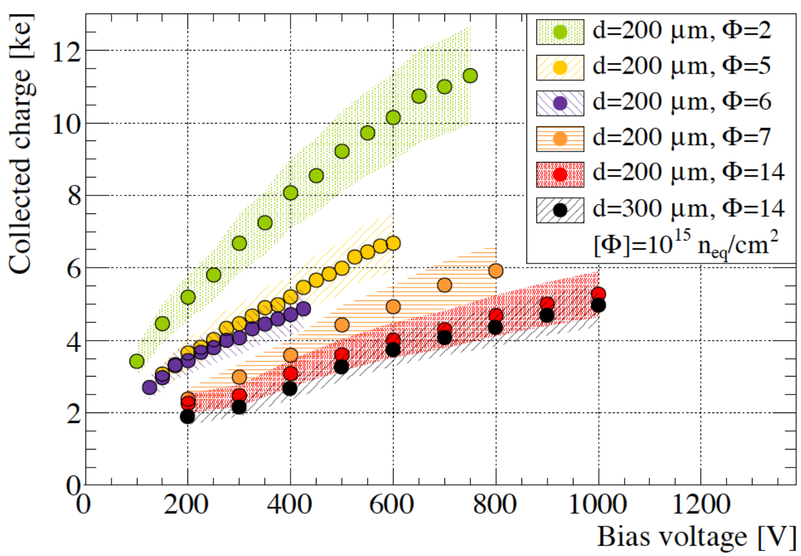
Charge collection properties of thin n-in-p pixel sensors

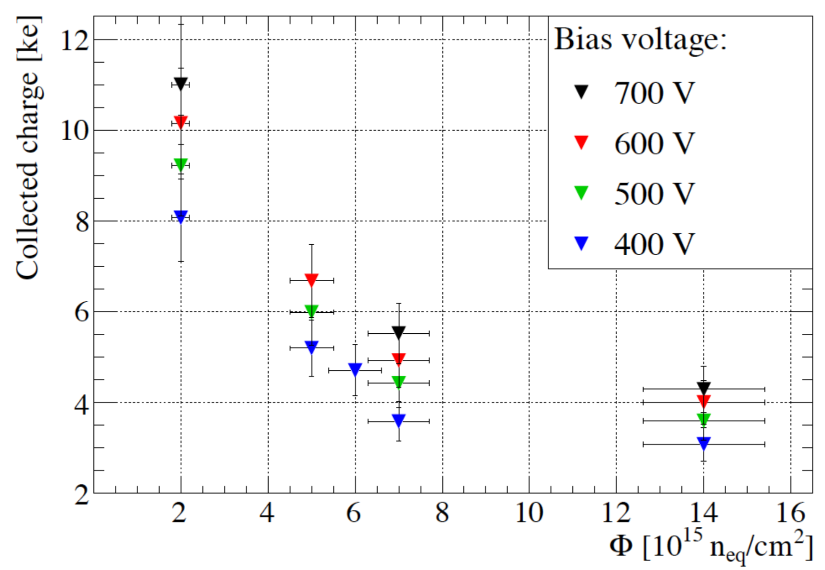
Charge collection after irradiation for 100 μm thin sensors





Charge collection after irradiation for 200 μm thin sensors





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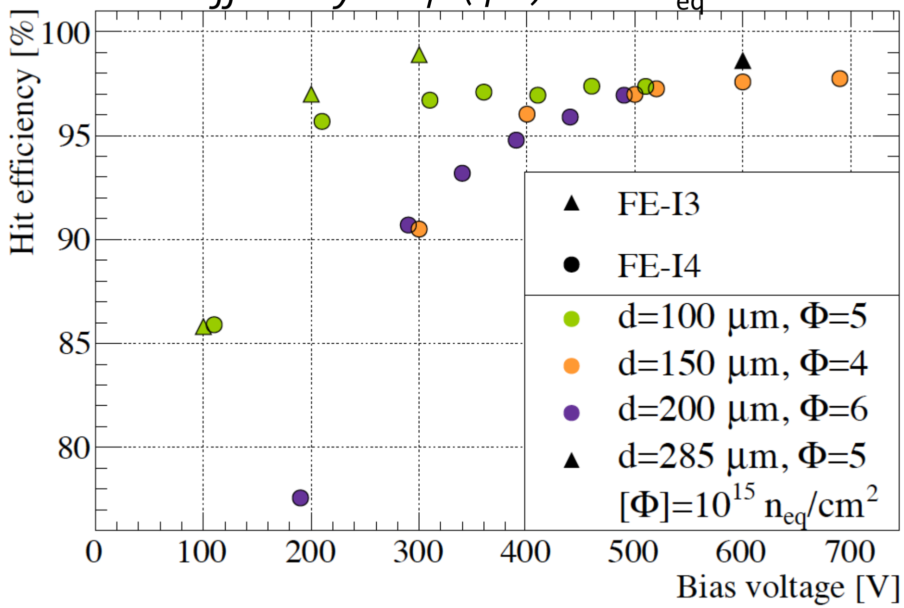
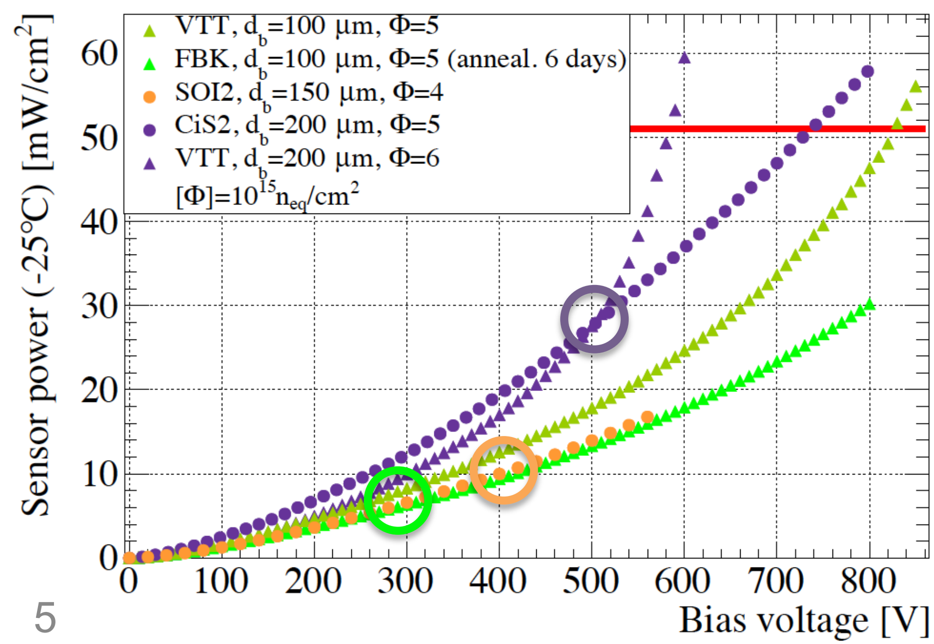
Pixel performance as a function of thickness

Hit efficiency at ϕ=(4-6) x10^{15} n$_{eq}$cm^{-2}



- With a radiation fluence between 4 and 6 x10^{15} n$_{eq}$cm^{-2} FE-I4 modules with 150 and 200 µm thick reach hit efficiencies of about 97% at Vb=500V
- FE-I4 modules with 100 µm with thick sensors start to saturate to this value already at Vb = 250-300V.

Power dissipation at ϕ=(4-6) x10^{15} n$_{eq}$cm^{-2}



Lower operational bias voltages result for thinner sensors in an improvement in the power dissipation performance

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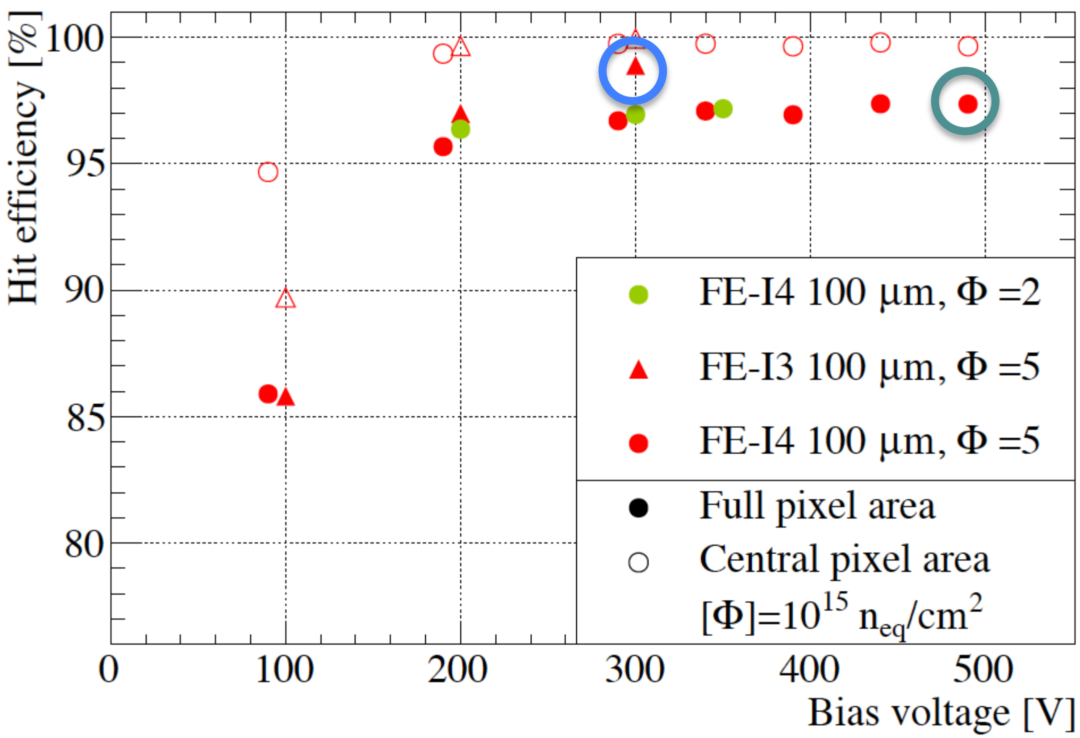
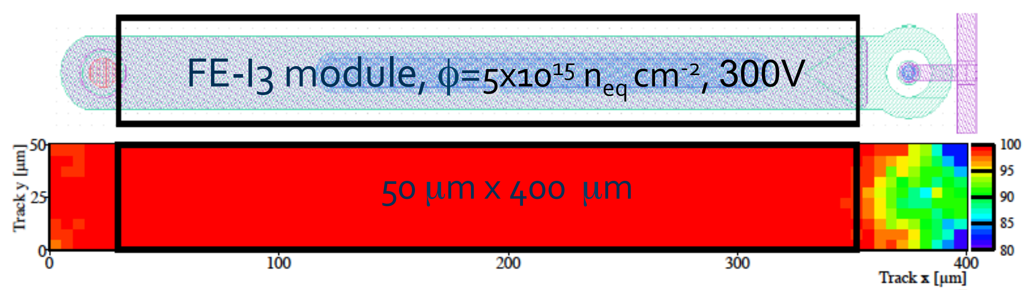
Limiting effects on hit efficiency at high fluence



- Hit efficiency measured with ADVACAM sensors, 100 μm thin, interconnected to FE-I3 and FE-I4 chips
- Average hit efficiency lower for FE-I4 compatible sensors with respect to FE-I3, due to the fact that the Punch Through Structure occupies a higher fraction of the pixel cell area

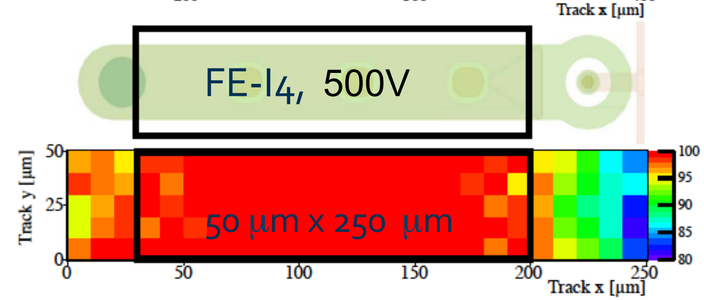
Beam test at CERN-SPS

with 120 GeV pions

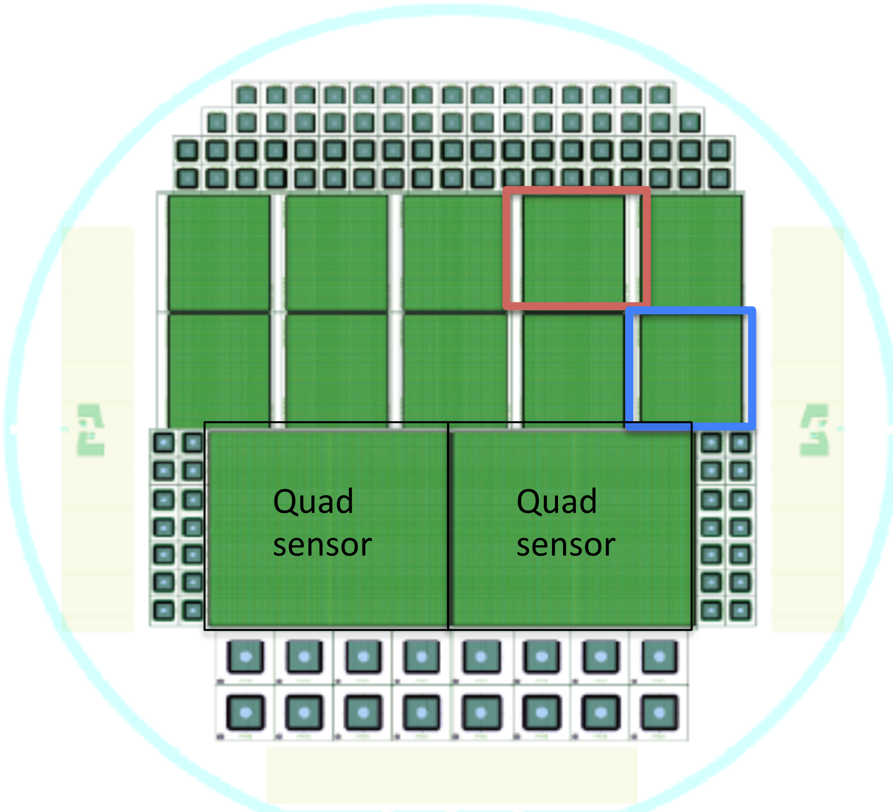


Beam test at DeSY

4 GeV electrons



Production of n-in-p pixels on 6" wafers at CIS



- First 6" wafer production at CIS on p-type material, 16 kΩ cm
- Wafer thickness 265-270 μm (thinning and polishing performed at Rockwood)
- FE-I4 Single chip sensors with different cell design plus FE-I4 quad modules

Project partially funded by RD50

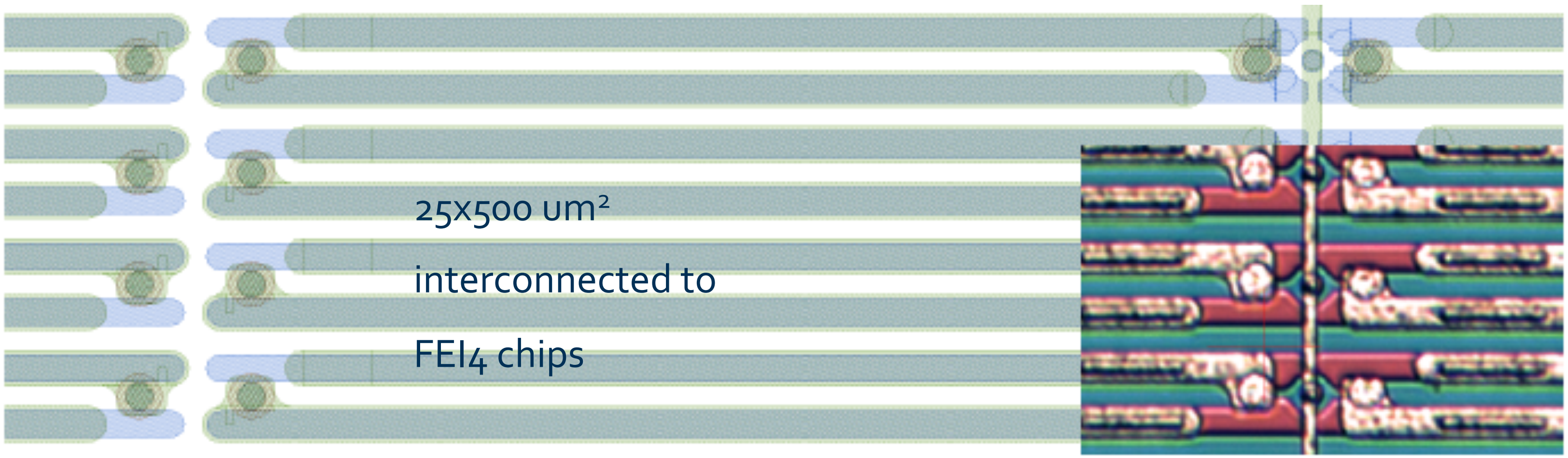
FE-I4 sensor with three different punch-through structures implemented in groups of 10 columns, standard pitch 50 μm x 250 μm

- BCB coating for sensor-chip isolation and interconnection to FE-I4 chips performed by IZM-Berlin

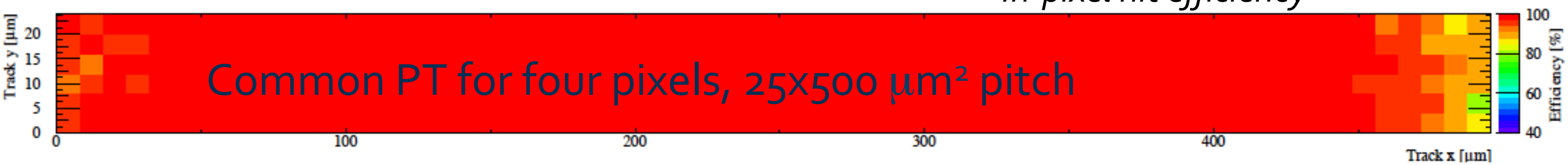
FE-I4 sensor with punch-through structure common to four pixels, pitch 50 μm x 250 μm

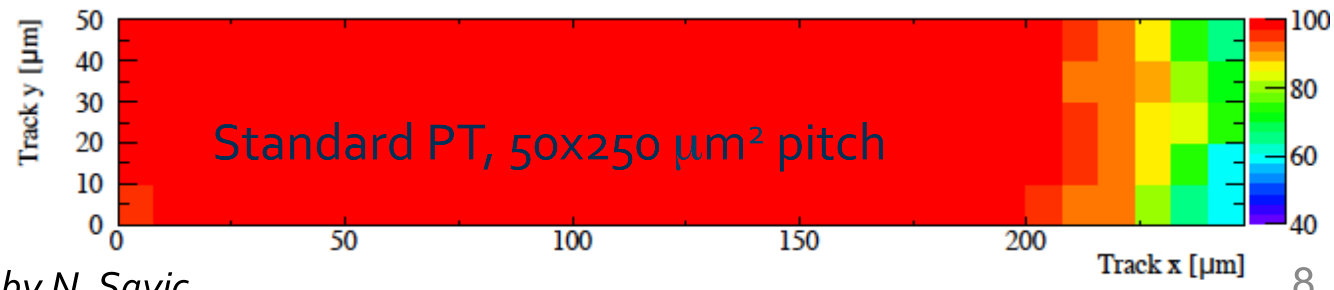
Optimization of the Punch Through Structure

- Results of beam test performed at DESY with 4 GeV electrons
- Single chip module irradiated at KIT with 25 MeV protons at a fluence of $3x10^{15}$ n_{eq} cm^{-2}
- Common punch-through structure to four pixels optimized for small pitches



In-pixel hit efficiency

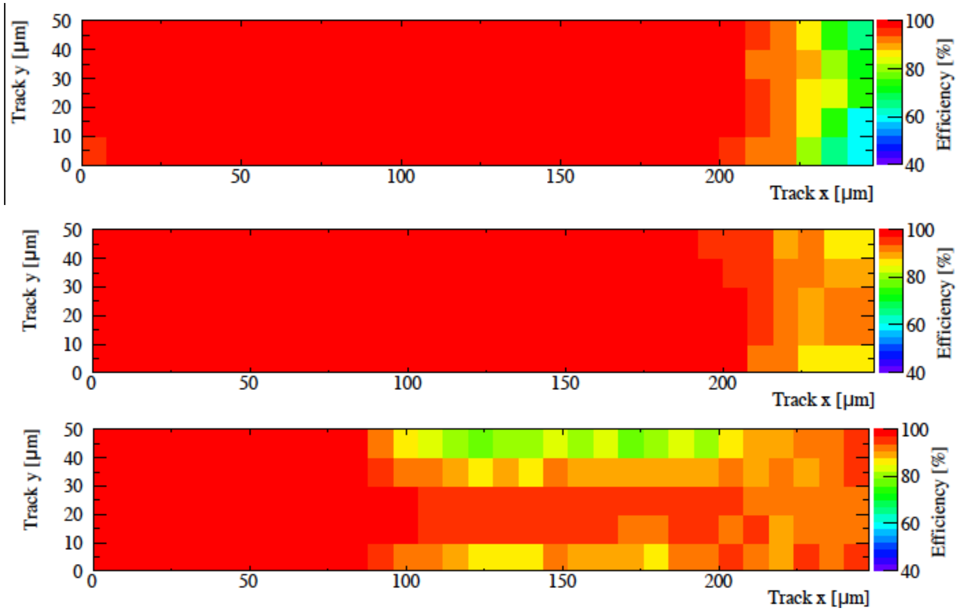


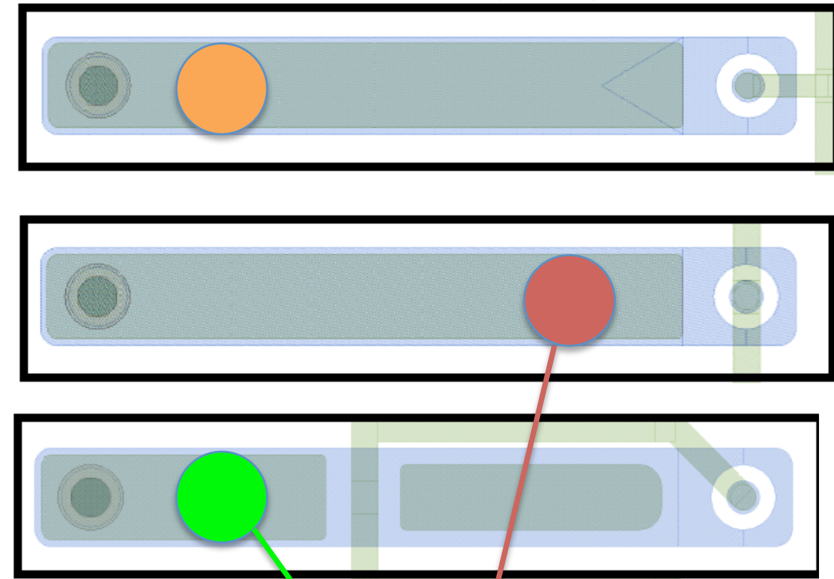


Test-beam data analysis by N. Savic

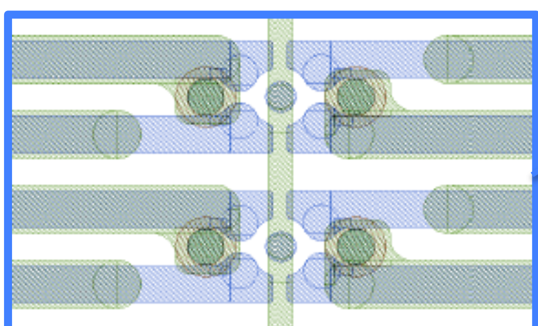
Optimization of the Punch Through Structure (II)

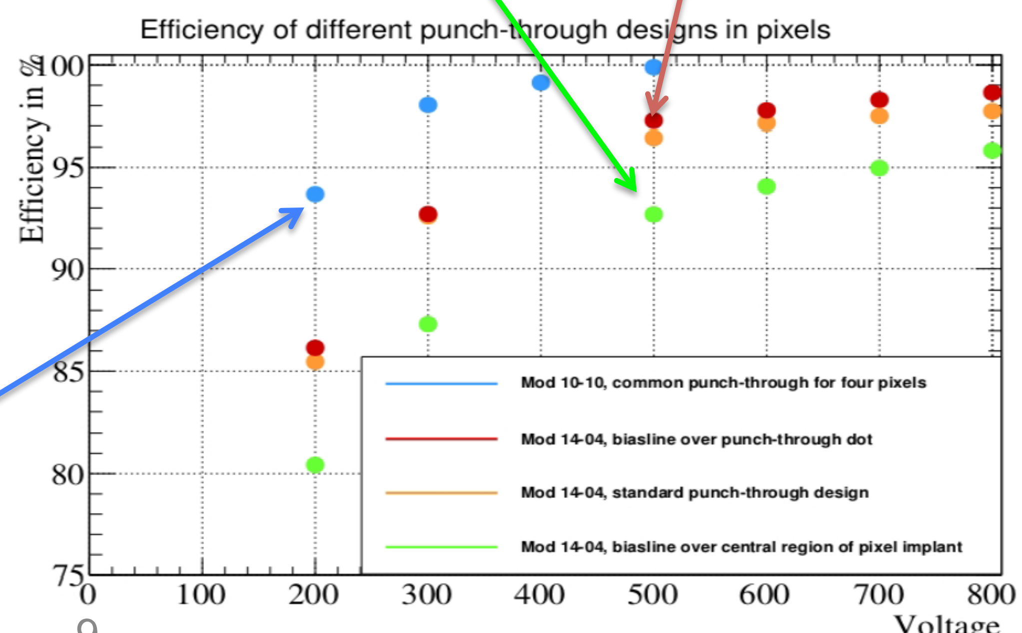
Test-beam data analysis by N. Savic





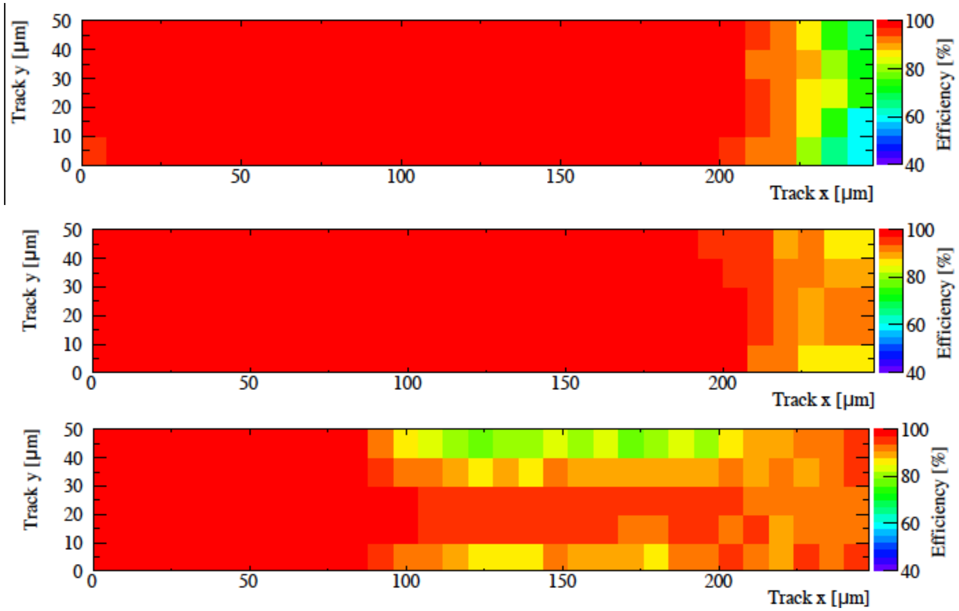
- Comparison of performance of different punch-through designs
- CIS3 sensors (270 um thick) irradiated at 3e15 at KIT

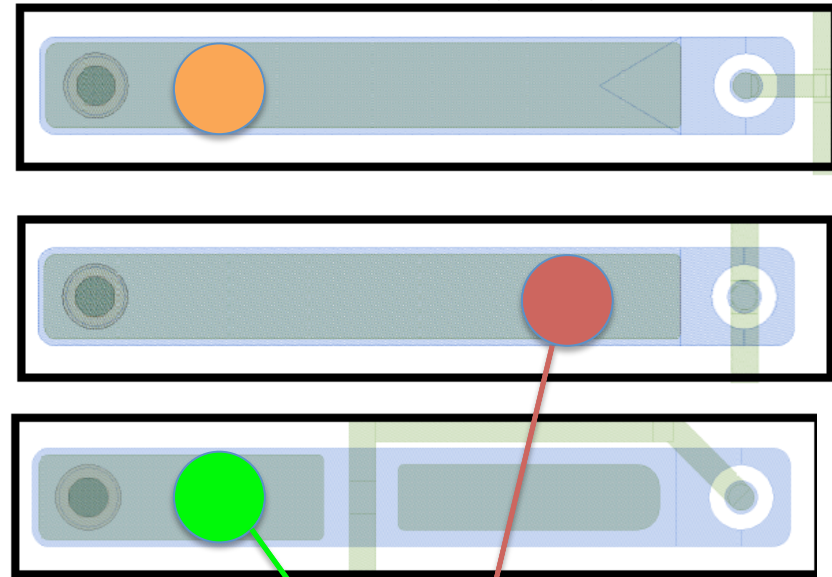




Optimization of the Punch Through Structure (II)

Test-beam data analysis by N. Savic





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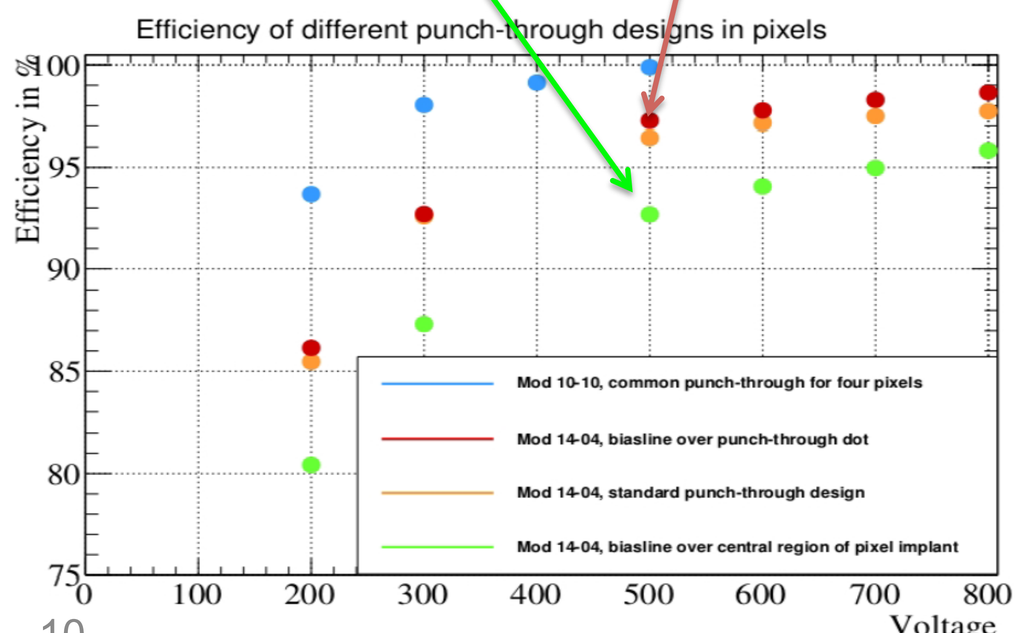
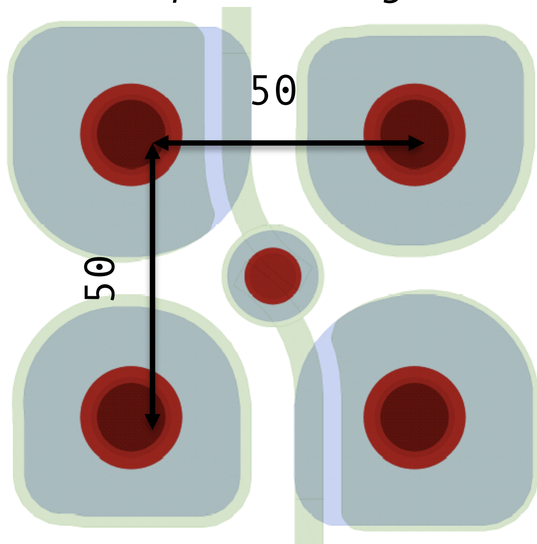


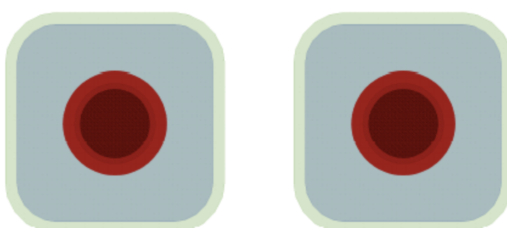
Highest eff. common PT

at 500V (99.4 ± 0.3)%

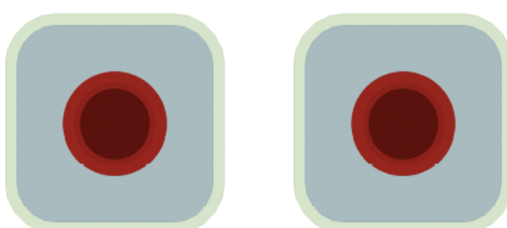
New design for sensors compatible with the RD53 chip

Common punch-through





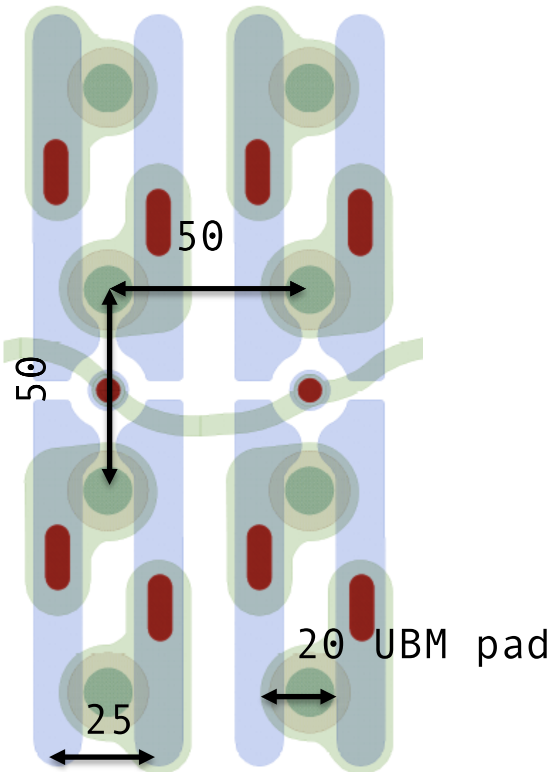
No bias rail structure



- New read-out chip for the future generation of pixel modules developed by the RD53 Collaboration
- 50 μm x 50 μm pitch for the chip, probably with bumps placed on a regular grid

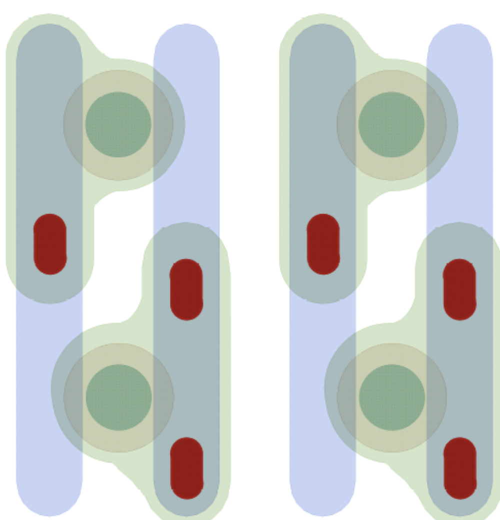
- Two different versions of sensors for RD53A chip with 50 μm x 50 μm pitch:
  - Common punch – through with bias rail running over implants to minimize hit efficiency loss after irradiation
  - Without any bias rail structure

Sensors compatible with 65 nm CMOS

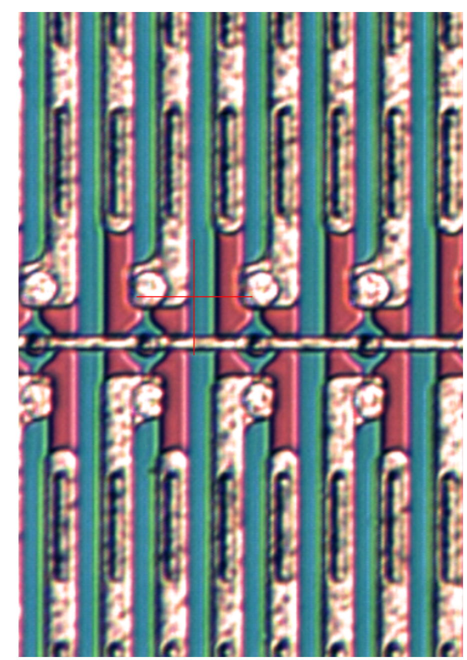


25x100 μm^2 pitch

- Pixel staggered in such a way to be compatible with a regular 50x50 μm^2 grid on the chip side
- Still realizable with a standard UBM size = 20 μm
- Design based on an existing prototype produced at CIS with 25 x 500 μm^2 pitch, FE-I4 compatible



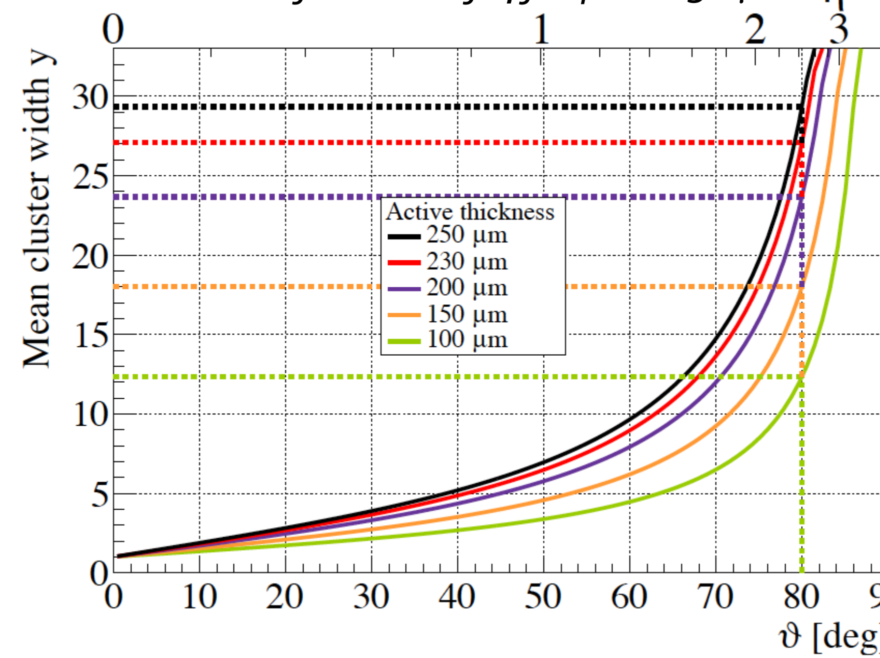
- No increase of cross-talk observed in 25x500 μm^2 FE-I4 compatible sensors:
  - direct measurements with ATLAS RCE read-out system
  - Analysis of cluster size in beam test data



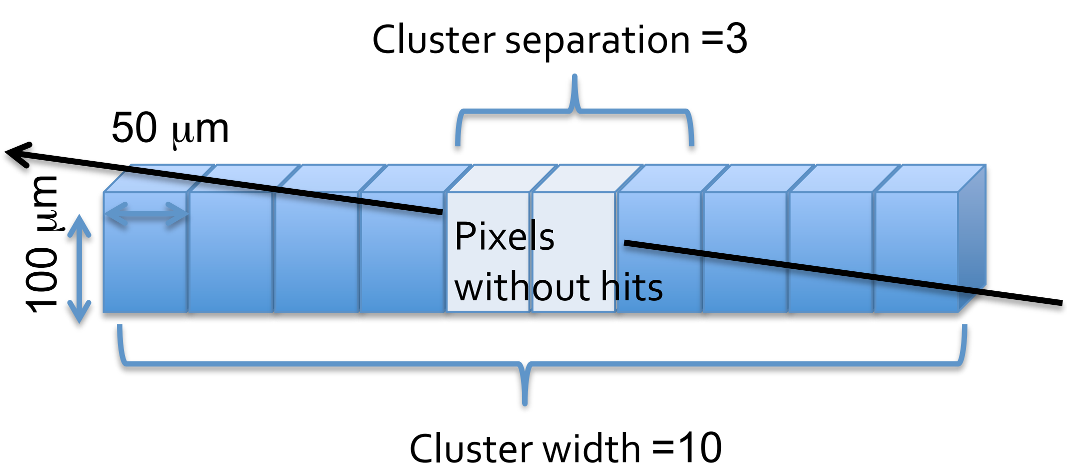
Hit efficiency for 50 μm pitch at high pseudo-rapidity

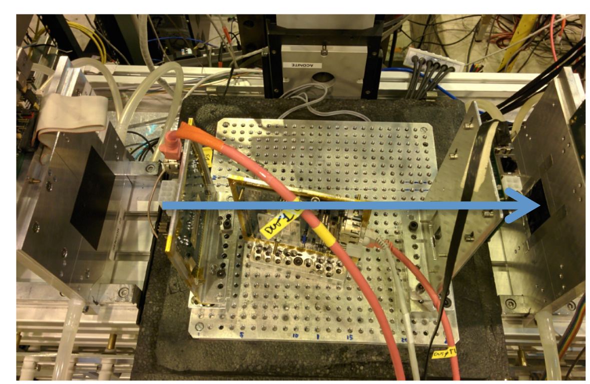
- Aim: study the performance of 50x50 μm² pitch sensors at high η
- Solution: use FE-I4 modules at high ϕ (80° → η=2.5) almost parallel to the beam but rotated by 90° with respect to their normal pixel orientation in the detector
- Samples: 100 μm thick planar sensor (VTT)
- No tracking information from EUDET telescope used (problems encountered in reconstruction)

Cluster width as a function of η for pitch=50 μm

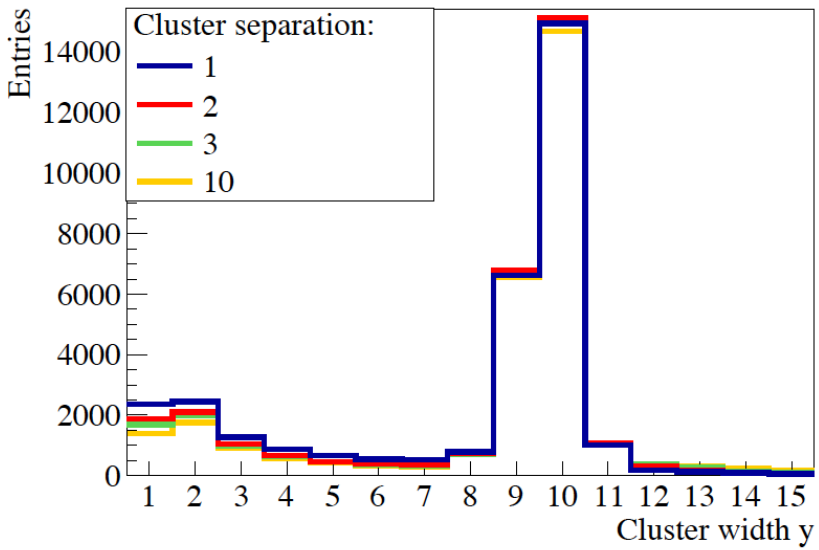


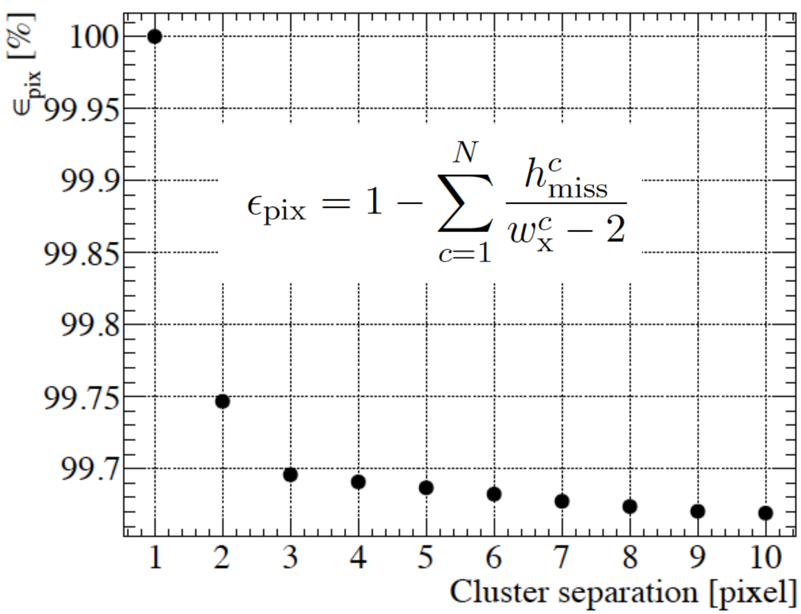
- Very long cluster expected along z for high ϕ = 80° (η=2.5), use them as "tracks"





Performance at high η: Cluster Multiplicity



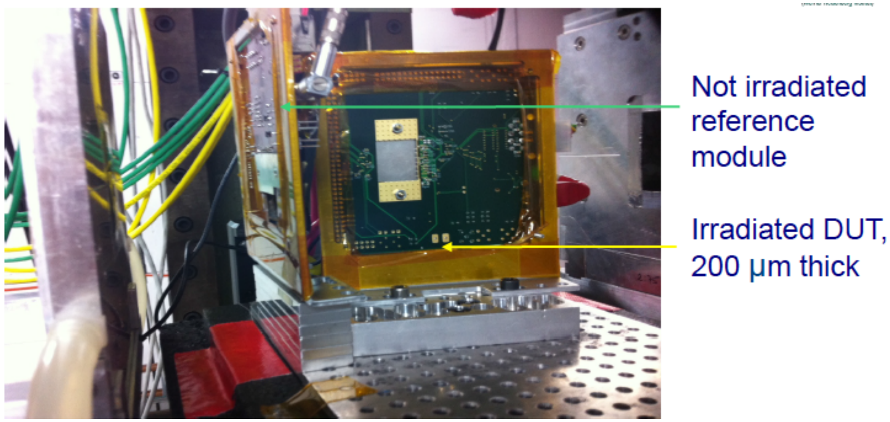


- Module Tuning:
  - Threshold 1 ke (planar, 3D), 1.5 ke (3D)
  - Charge calibration 6 ToT at 4 ke
- Measured cluster width in Y (along 50 μm pitch direction) 2-3 units less than pure geometrical expectations
- Difference is due to ~ 1 degree misalignment and threshold effects in the entrance and exit pixels

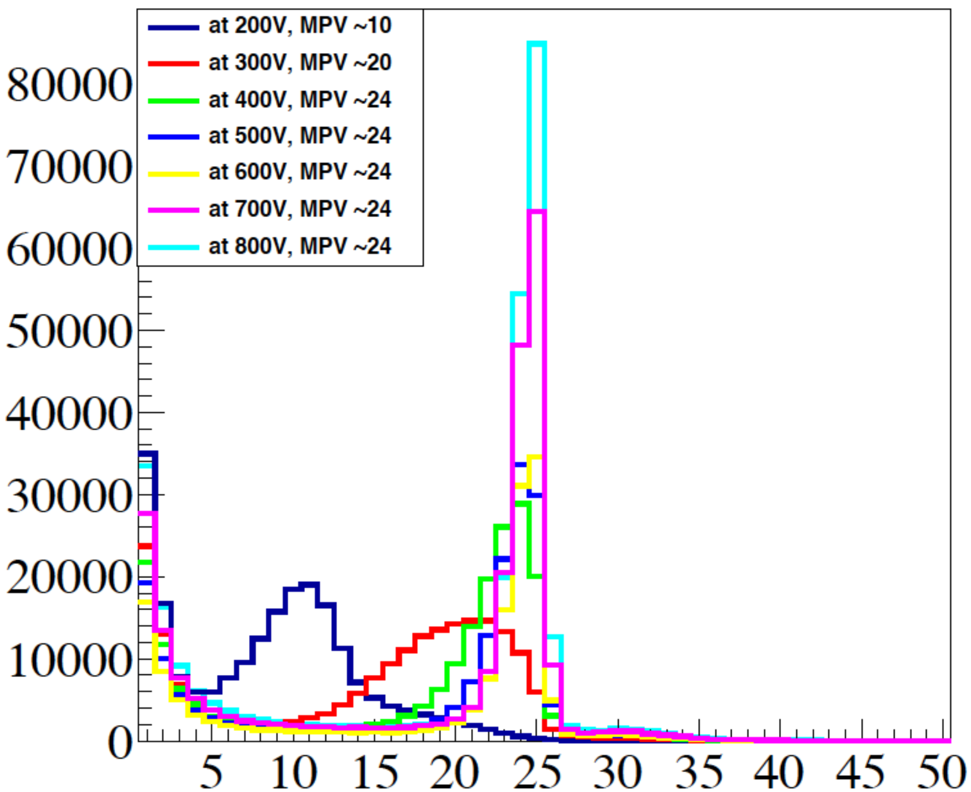
Good single hit efficiency with 100 μm thin sensors with 50 μm pitch:

(99.6-99.7)%

Performance at high pseudo-rapidity after irradiation (I)

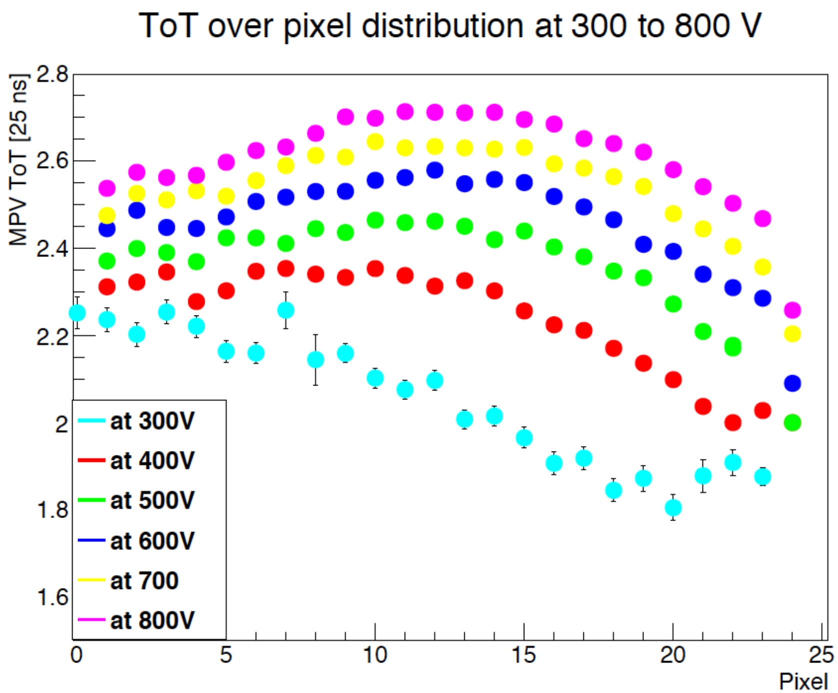


- Study the performance of planar pixel modules after irradiation in a beam test at DESY with 4 GeV electrons
- FE-I4 module, CIS production, irradiated to a fluence of 2×10^{15} n_{eq} cm^{-2}
- Same inclination as not-irradiated one, high $\phi = 80^{o}$ (η=2.5)

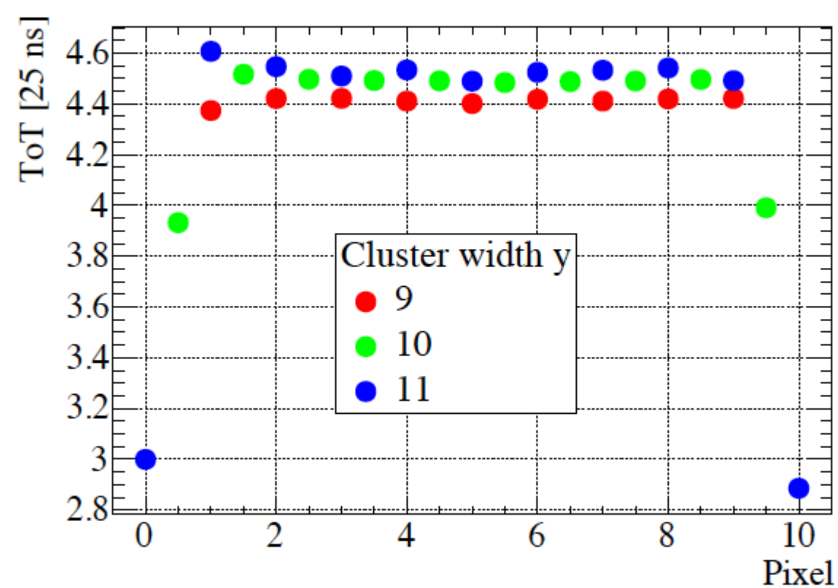


- Cluster width distribution from 200V to 800V
- Expected cluster size from geometry ~24 → due to the double sensor thickness than in the previous study
- Maximum separation of 10 pixels allowed in the analysis

Performance at high η after irradiation (II)

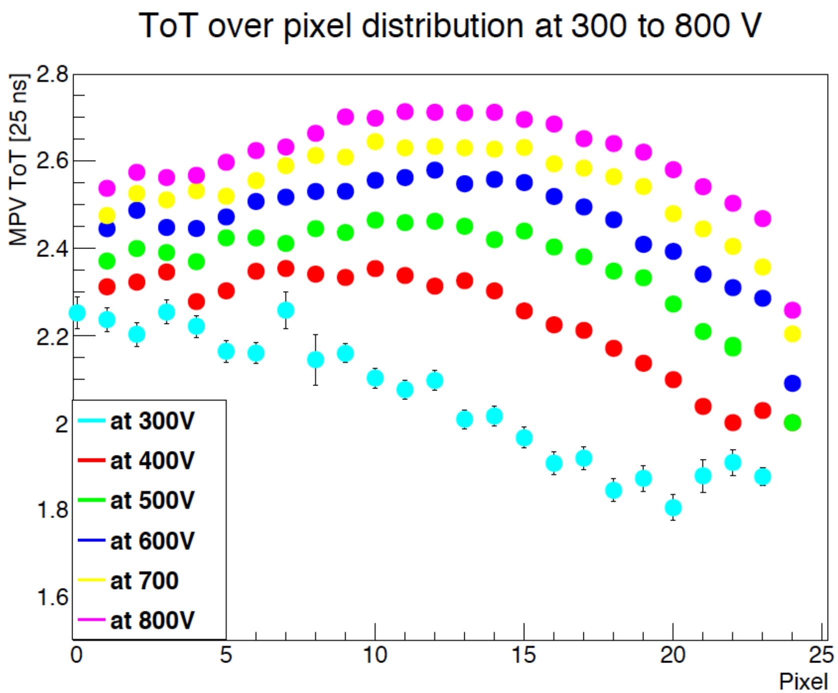


- Grazing angle technique is also a powerful method to investigate charge collection at different depths of irradiated sensors
- Charge collection vs pixel number and depth at 300 V up to 800 V for a cluster width of 24
- Module tuned with a threshold of 1000e



- Before irradiation constant charge is observed at different depths except for the entrance and exit pixels, where pixels are only partially crossed

Performance at high η after irradiation (III)



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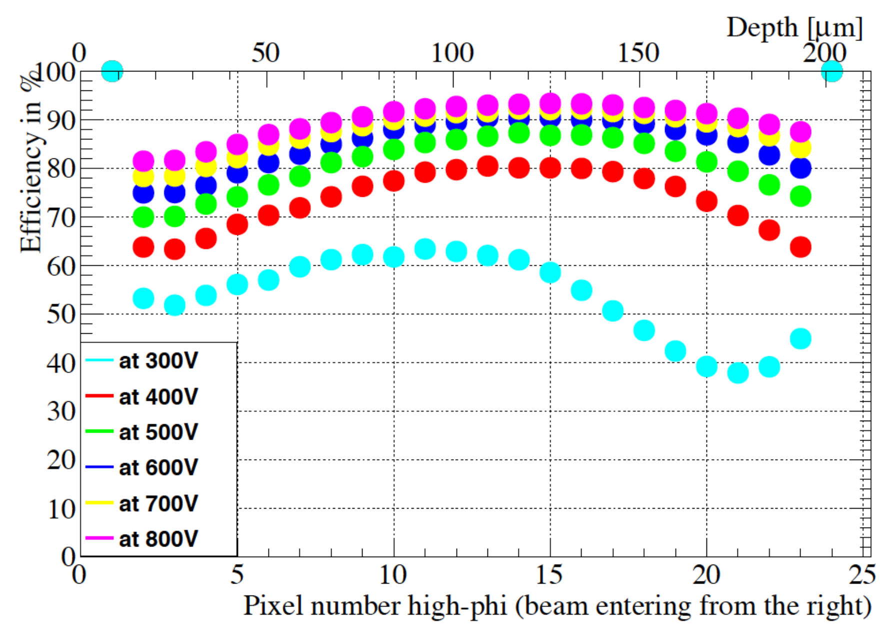
- Charge collection vs pixel number and depth at 300 V up to 800 V for a cluster width of 24
- Module tuned with a threshold of 1000e

- Single pixel hit efficiency for cluster size=24 at different bias voltages
- Maximum separation allowed = 10 pix.
- (81.5-93.4)% single hit efficiency for the highest bias voltage in the full depth range.

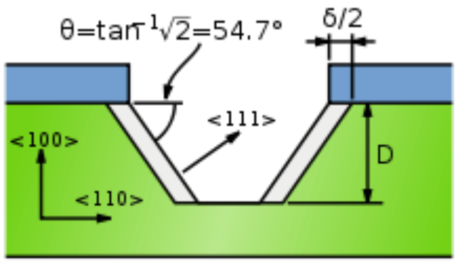


On-going productions of thin n-in-p pixel sensors

- Explore the thickness range 50-150 μm to investigate the optimal thickness for the different pixel layers
- Compare different processing methods
- Test new pixel cell designs with common PT structures

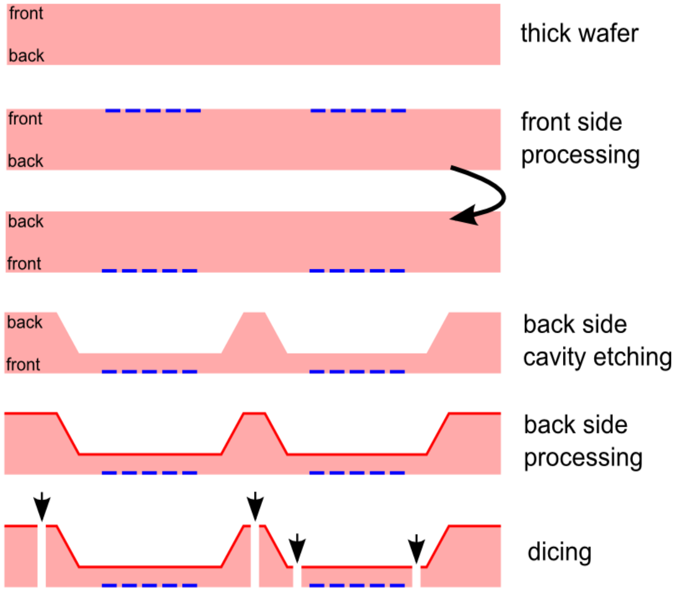
New thin production at CIS - Technology

- relatively simple technology without using support / handling wafers
  - anisotropic wet etching (KOH) on <100> wafers
  - Experience with this technology at CIS for MEMS/ pressure sensors production



- First R&D production on 4" p-type FZ wafers; process contributed by CIS**; target thickness 100 and 150 µm**

- Starting thickness 525 µm
- Front-side processing up to nitride deposition and patterning
- Back-side p+ implantation, top-side p-spray → common annealing step
- Metallization on the front and back side
- UBM (electroless Nickel at CiS or standard one at IZM)
- dicing



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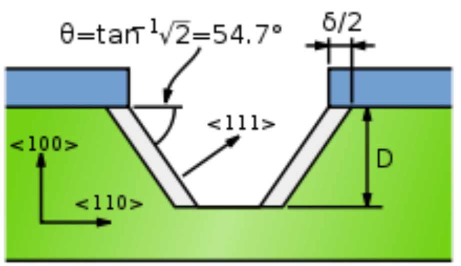
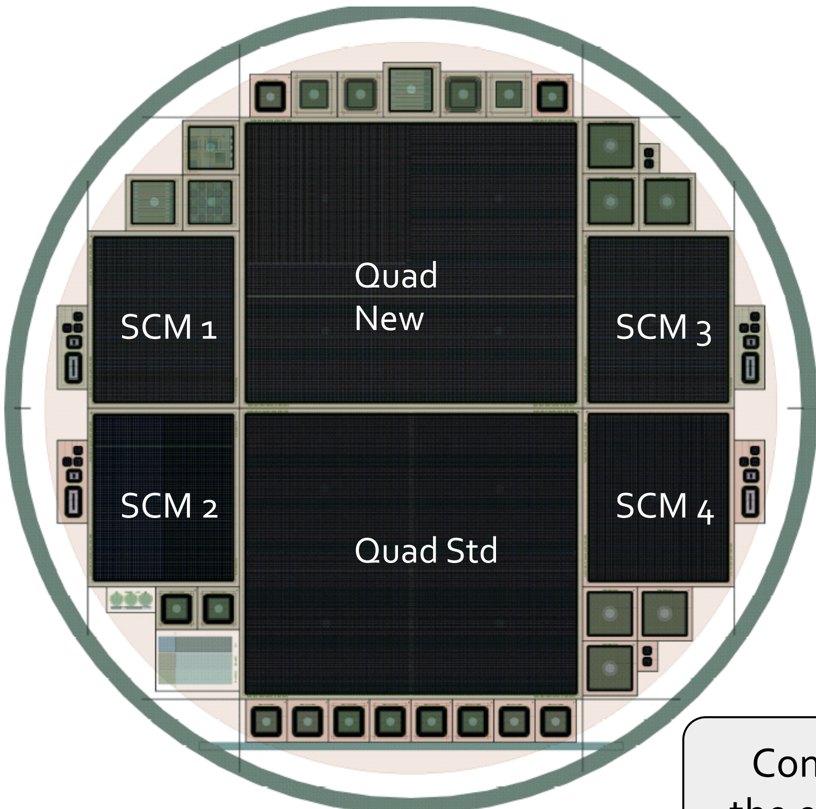
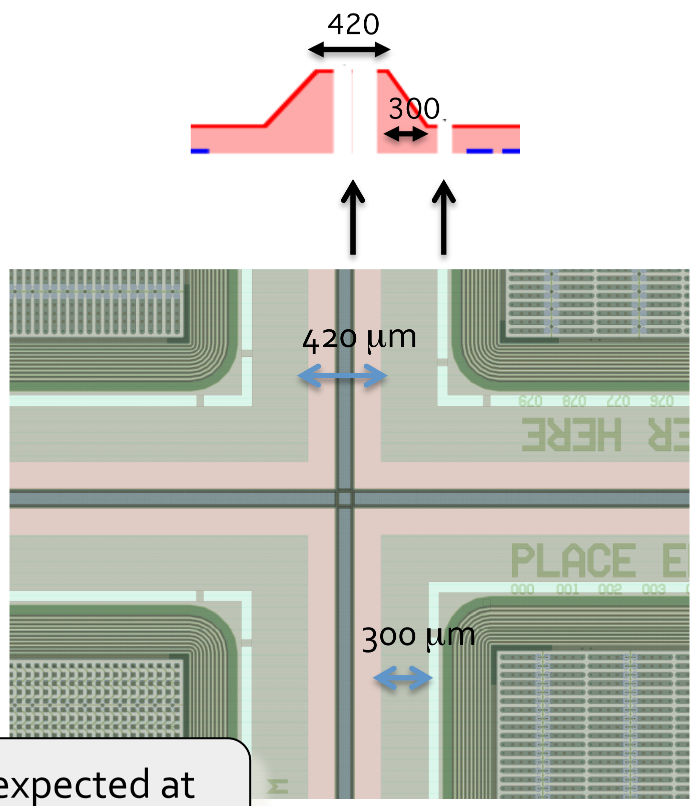


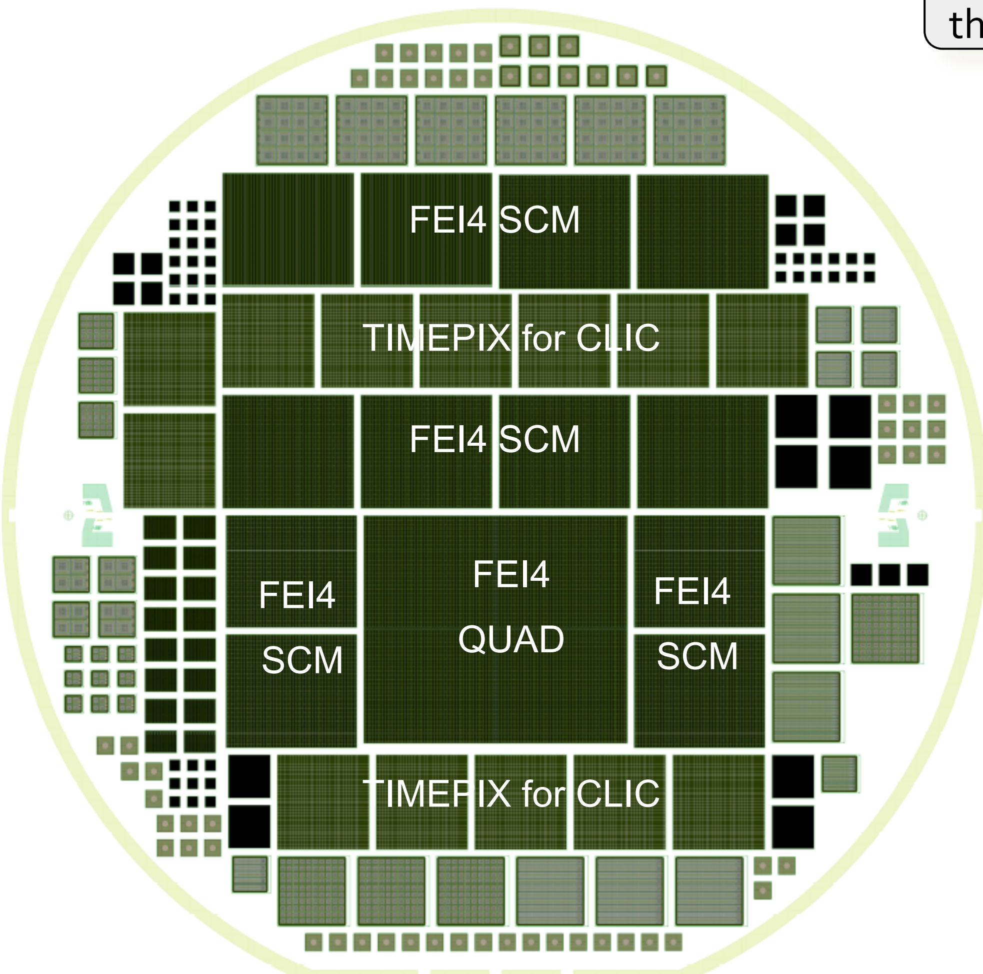




Completion expected at the end of November 2015

Second production of active edge pixels at ADVACAM

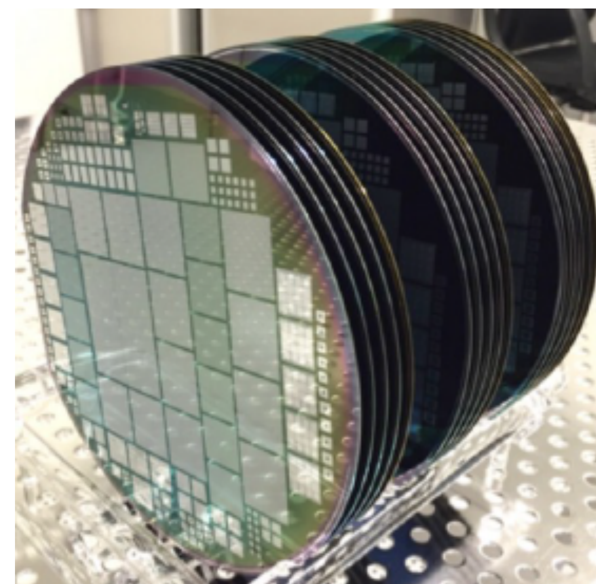
Wafer layout of the new production



6" SOI wafers: active edge process for all the structures

- In collaboration with Glasgow, Göttingen, LAL, CLIC CERN-LCD,
- Geneva University for medical applications

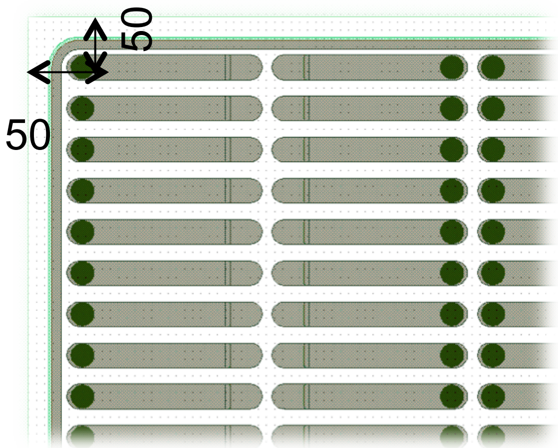
50, 100, 150 μm sensor thickness: 5 FZ p-type wafers for each thickness



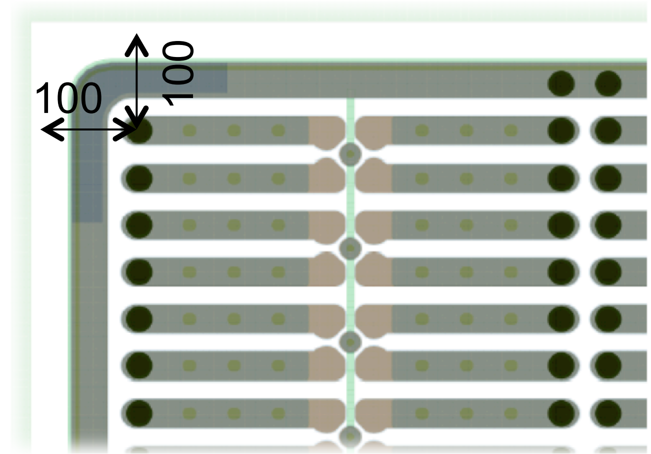
ADVACAM
Imaging the Unseen

FE-I4 Single Chip Modules

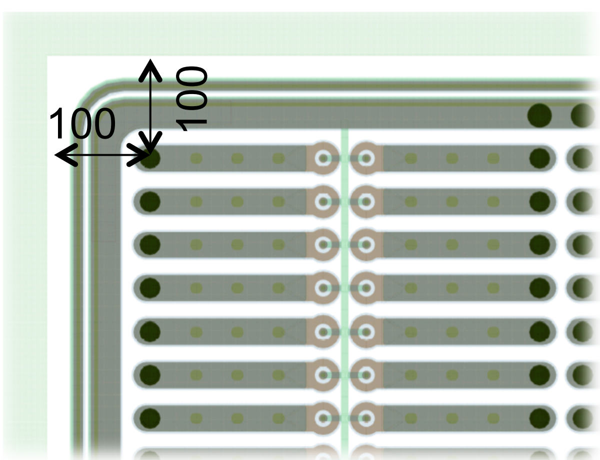
FE-I4 with 50 μm edge, one GR,
no punch-through structure



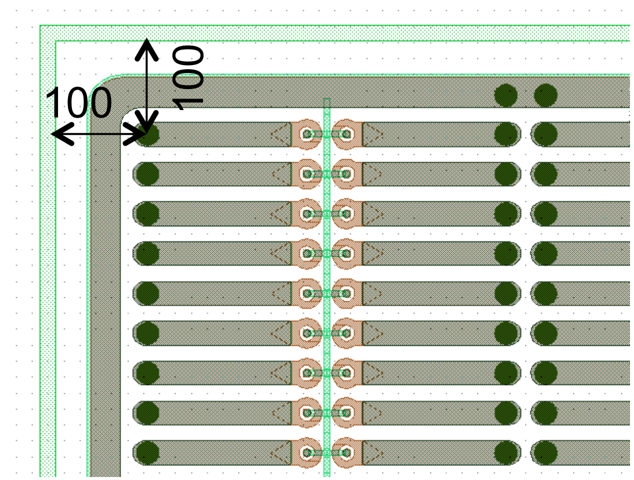
FE-I4 with 100 μm edge, Bias Ring,
new external punch-through structure



FE-I4 with 100 μm edge, Bias Ring + Guard Ring, std punch-through structure



FE-I4 with 100 μm edge, Bias Ring,
std punch-through structure



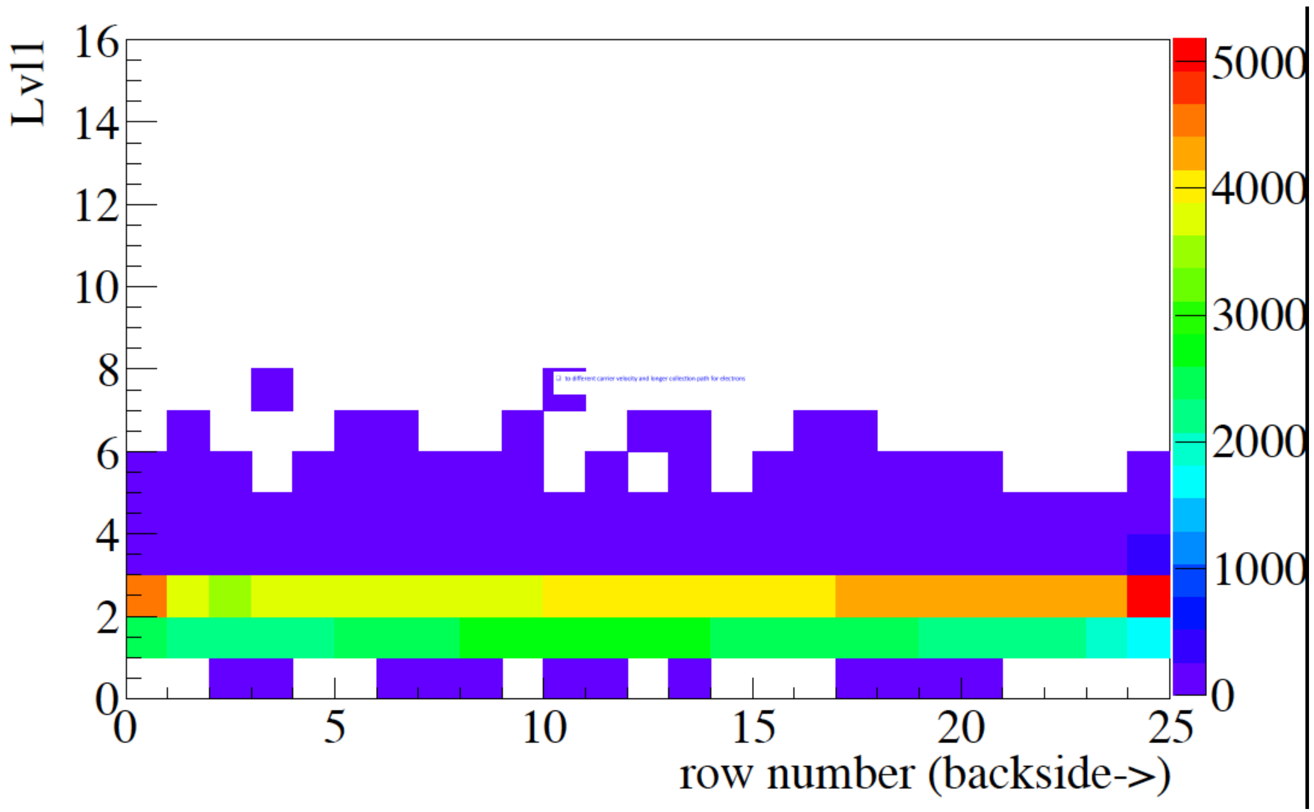
Summary and Outlook

- Excellent performance of thin n-in-p pixel sensors demonstrated before and after irradiation up to a fluence of $5x10^{15}$ n_{eq} cm^{-2}
- Design of pixel sensors compatible with RD53 chip has been optimized based on beam test analysis of different biasing structures
- Tracking with 50x50 μm^2 pitch at high eta investigated by using FE-I4 pixel modules at high-ϕ before and after irradiation. This technique also provides a tool to study charge collection at different depths in the silicon bulk
- On-going productions of thin n-in-p pixel sensors to expand the irradiation and testing program up to a fluence of 10^{16} n_{eq} cm^{-2}

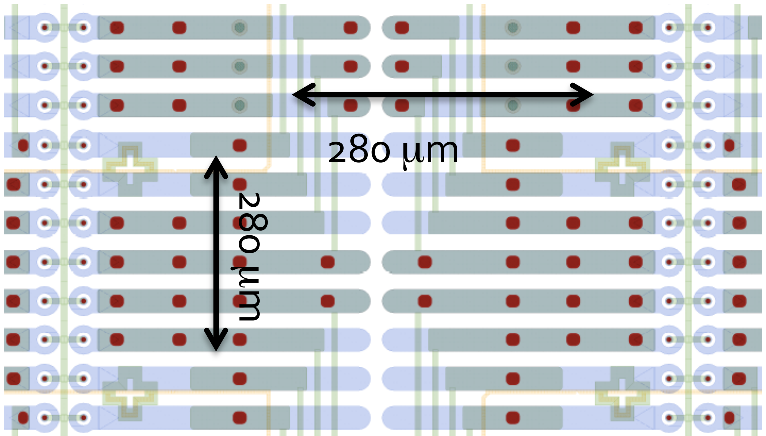
Additional material

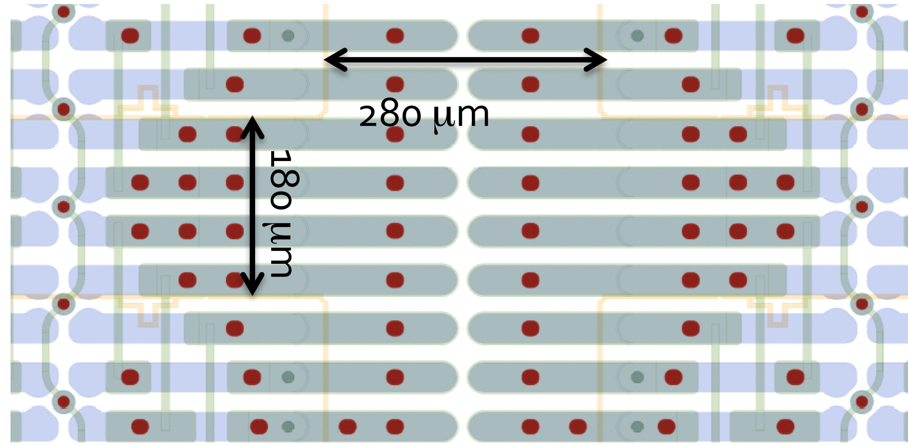
Possible effects of timing on charge distribution

- Charge collection properties at different depths probably slightly affected by time-walk effects due to different carrier velocity and longer collection path for electrons
- Slower signals close to the backside causes later crossing of pixel threshold and a decrease of ToT values → this is also visible in a higher average value of the Level1 distribution close to the backside (delay in unit of 25 ns with respect to the trigger signal)



Quad sensors and SCMs

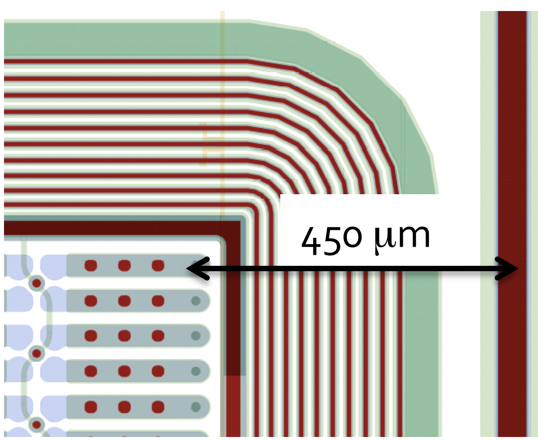


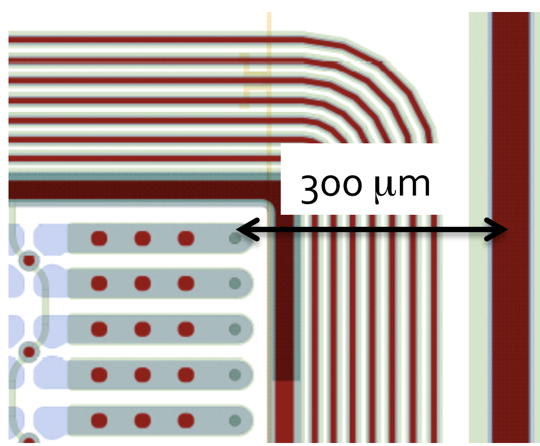


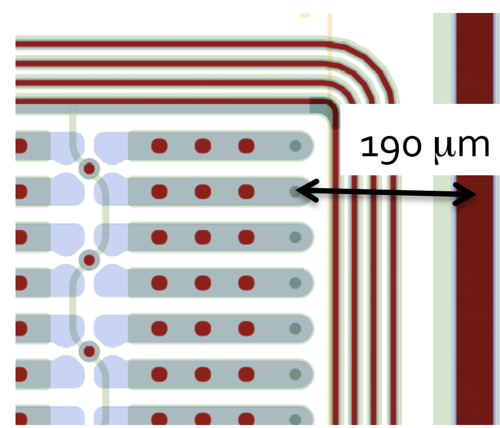
- 4 rows of ganged pixels
- Standard punch-through structures

- 3 rows of ganged pixels
- Common punch-through structures for 4 pixels

- FE-I4 SCM with reduced GR structures

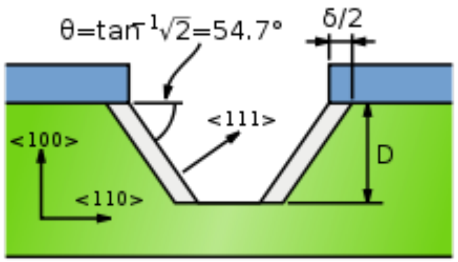






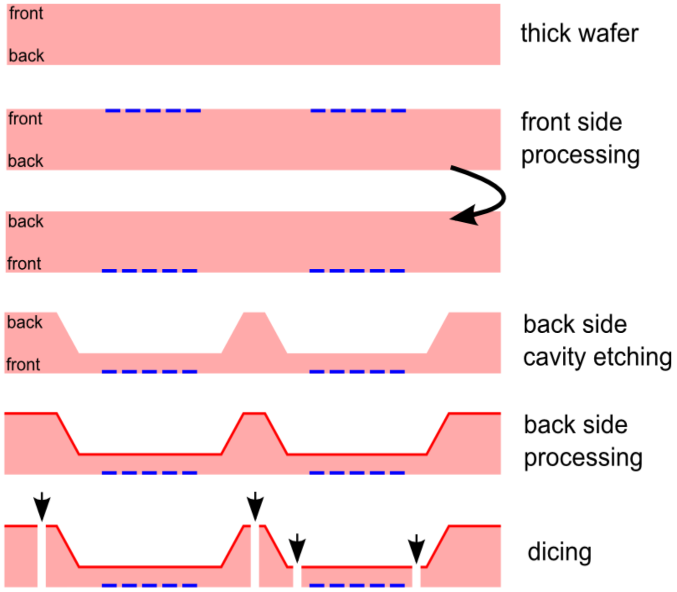
New thin production at CIS - Technology

- relatively simple technology without using support / handling wafers
  - anisotropic wet etching (KOH) on <100> wafers
  - Experience with this technology at CIS for MEMS/ pressure sensors production



- First R&D production on 4" p-type FZ wafers; process contributed by CIS**; target thickness 100 and 150 μm**

- Starting thickness 525 μm
- Front-side processing up to nitride deposition and patterning
- Back-side p+ implantation, top-side p-spray → common annealing step
- Metallization on the front and back side
- UBM (electroless Nickel at CiS or standard one at IZM)
- dicing



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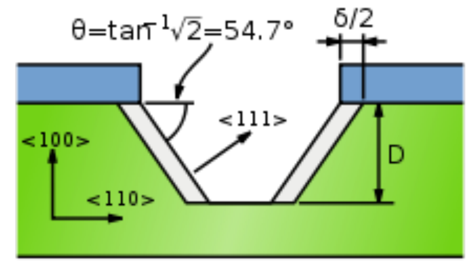
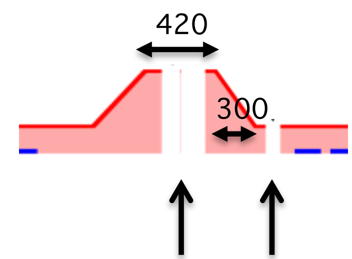
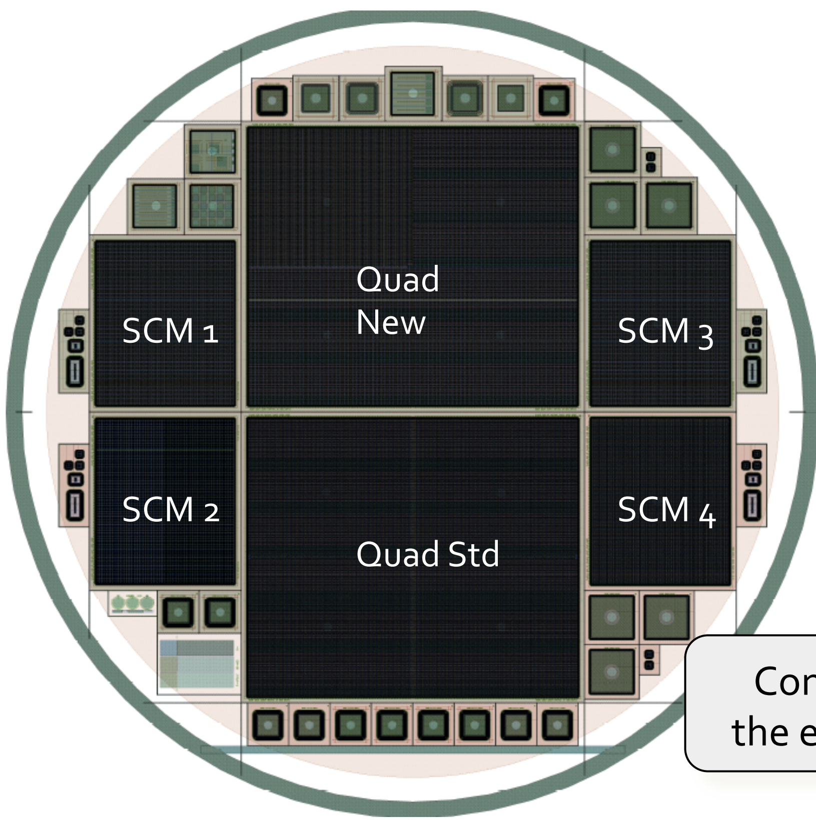
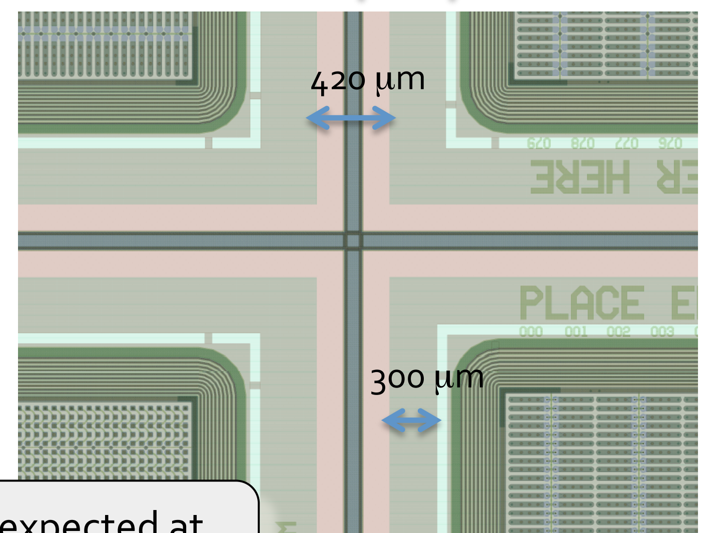


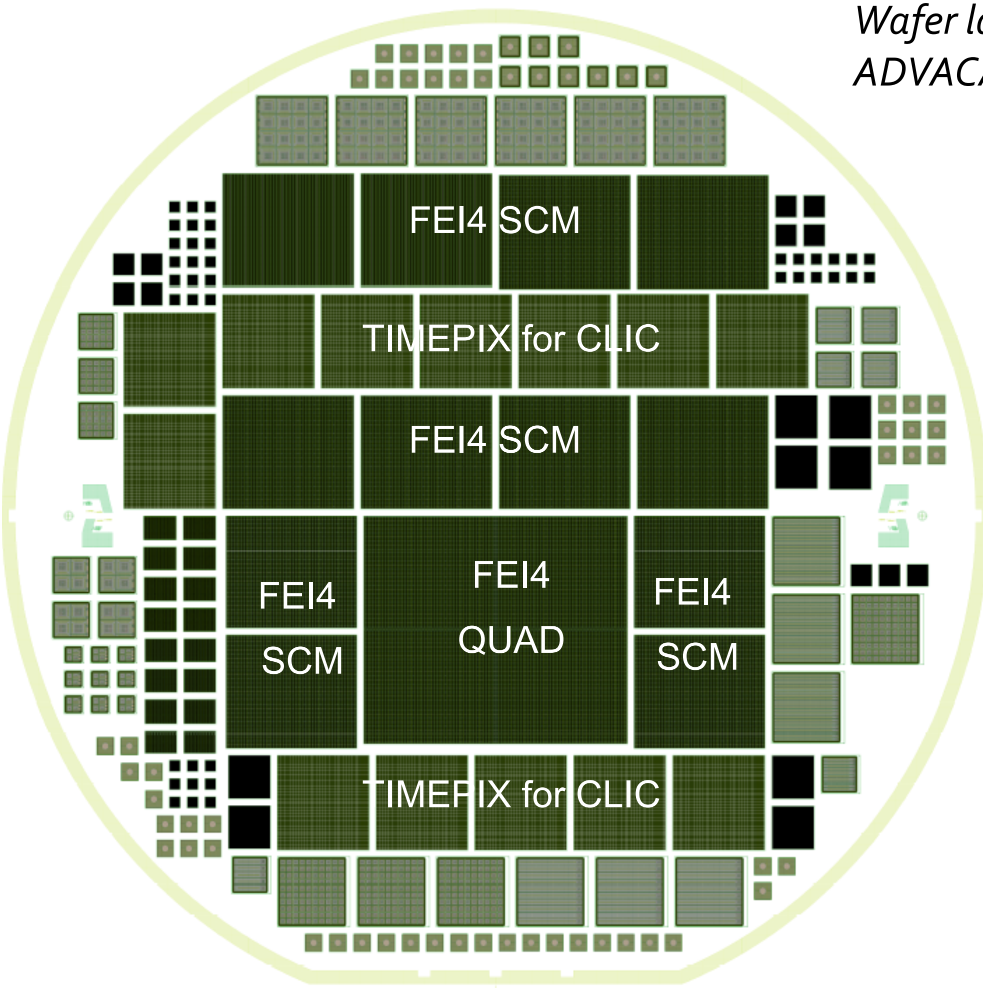






Completion expected at the end of November 2015

Second production of active edge pixels at ADVACAM

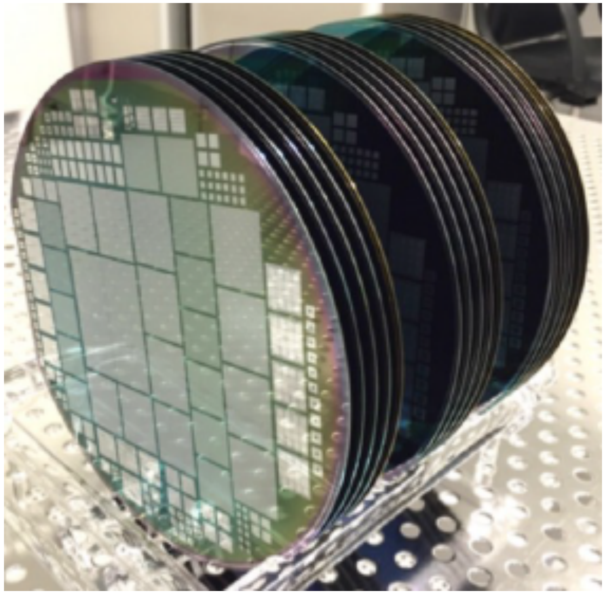


Active edge process for all the structures

Wafer layout of the new production at ADVACAM (spin-off VTT)

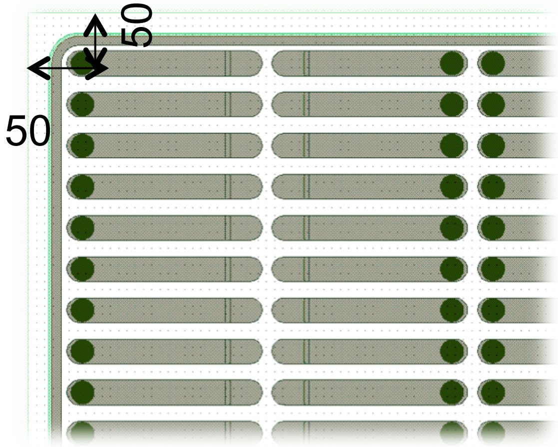
- In collaboration with Glasgow, Göttingen, LAL, CLIC CERN-LCD,
- Geneva University for medical applications

50, 100, 150 μm sensor thickness: 5 FZ p-type wafers for each thickness

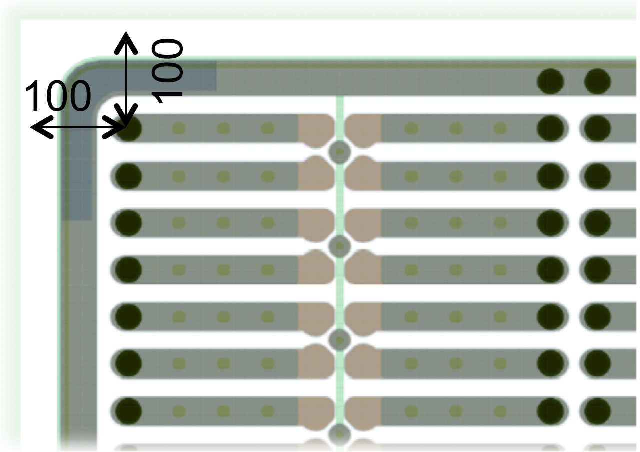


FE-I4 Single Chip Modules

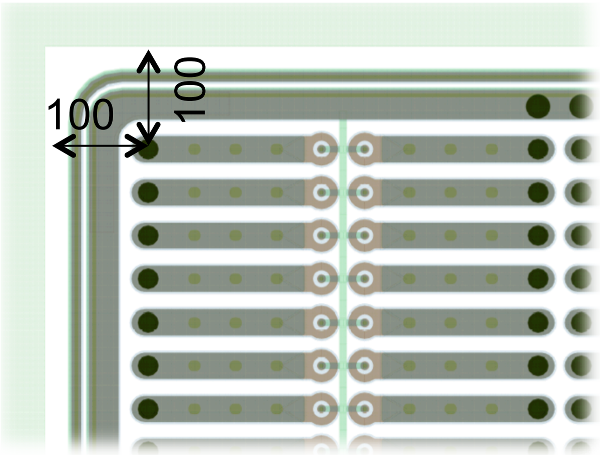
FE-I4 with 50 μm edge, one GR, no punch-through structure



FE-I4 with 100 μm edge, Bias Ring, new external punch-through structure



FE-I4 with 100 μm edge, Bias Ring + Guard Ring, std punch-through structure



FE-I4 with 100 μm edge, Bias Ring, std punch-through structure