

Towards AGIPD1.0: optimization of the dynamic range and investigation of a pixel input protection

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Towards AGIPD1.0: optimization of the dynamic range and investigation of a pixel input protection

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ABSTRACT: AGIPD is a charge integrating, hybrid pixel readout ASIC, which is under development for the European XFEL [1, 2]. A dynamic gain switching logic at the output of the preamplifier (preamp) is used to provide single photon resolution as well as covering a dynamic range of at least $10^4 \cdot 12.4$ keV photons [3, 4]. Moreover, at each point of the dynamic range the electronics noise should be lower than the Poisson fluctuations, which is especially challenging at the points of gain switching.

This paper reports on the progress of the chip design on the way to the first full-scale chip AGIPD1.0, focusing on the optimization of the dynamic range and the implementation of protection circuits at the preamplifier input to avoid pixel destruction due to high intense spots.

KEYWORDS: X-ray detectors; Instrumentation for FEL

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1 Introduction

The European XFEL will operate with $600\,\mu\text{s}$ long bunch trains, which are repeated at a rate of 10 Hz. The bunch trains are composed of 2700 bunches with a temporal separation of 220 ns corresponding to a rate of 4.5 MHz. The rate of incoming photon pulses requires the implementation of in-pixel storage cells, which will be read out in the 99.4 ms long pause between the bunch trains. One photon pulse consists of up to 10^{12} photons of 12.4 keV, of which up to 10^4 are expected to impinge on a single pixel quasi-simultaneously (< 100 fs). These given properties demand for a sophisticated detector design in order to fulfill the requirements of single photon resolution, as well as a dynamic range of at least $10^4 \cdot 12.4$ keV photons per pixel and having a noise performance, which is better than the Poisson limit at every point of the dynamic range.

AGIPD (*adaptive gain integrating pixel detector*) is facing these challenges with a charge integrating, hybrid readout ASIC (*application specific integrated circuit*), which will be bump bonded to a silicon sensor. A dynamic gain switching scheme is used in order to adapt the gain of the preamplifier to the number of incoming photons. A logic at the preamplifier output compares the output voltage with an adjustable threshold voltage and adds a 2nd and 3rd feedback capacitor, if needed [4]. This results in three different gain stages (high, medium and low). Single photon resolution will be achieved in the high gain range and the maximum dynamic range will be reached in the low gain range. The noise of the high gain stage has to be sufficiently low to be able to resolve single photons [8]. In order to ensure a noise performance which is better than the Poisson limit for the whole dynamic range, the readout chain, especially the preamplifier and CDS (*correlated double sampling*) stage need to be carefully designed and special care has to be taken sizing the feedback capacitors.

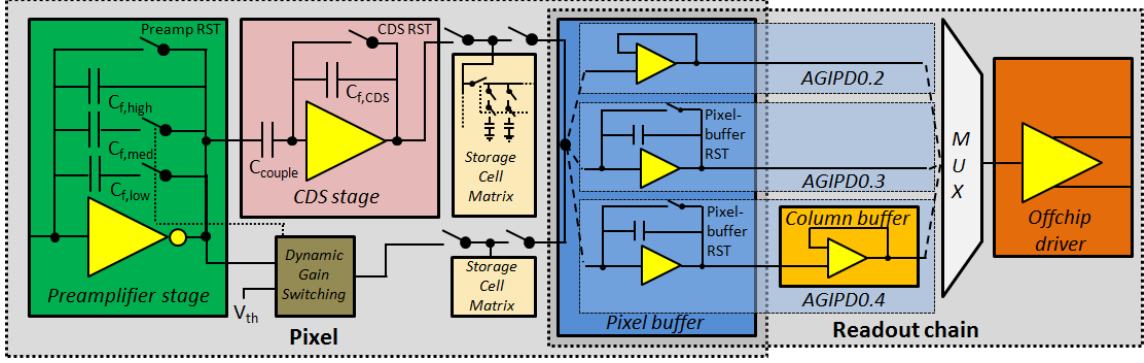


Figure 1. Simplified block diagram of the pixel architecture of AGIPD0.2 to AGIPD0.4.

Another challenging task is dealing with the extreme experimental environment AGIPD will be facing. A total ionizing dose of 1 GGy is expected to impinge on the sensor during 3 years of operation [5]. This dose requires radiation tolerant ASIC design techniques, even with the very deep-submicron CMOS technology used for the production of AGIPD (IBM 130 nm) [6, 7]. In order to protect the pixels against high voltage swings at the preamplifiers input due to high intensity spots, different protection circuits have been implemented at the input of the preamplifier ($V_a = 1.5$ V). They consist of either a diode or a NMOS switch, which are connected to an adjustable voltage at their backside.

This paper will give an overview of the status of the chip characterization, focusing on the dynamic range and the protection circuits and will give an outlook towards the expected performance of the first full-scale chip, AGIPD1.0, which was submitted in spring 2013.

2 Experimental setup

2.1 The AGIPD prototype chips

Four different prototype chips (AGIPD0.1 to AGIPD0.4) have been developed so far (Summer 2013). AGIPD0.2 to AGIPD0.4 feature a pixel matrix of 16×16 pixels with a pixel size of $200 \times 200 \mu\text{m}^2$ each. The chips were bump bonded to $320 \mu\text{m}$ thick silicon sensors, which were biased at $+120$ V. The specifications of the different revisions are summarized in ref [8]. A simplified block diagram of the AGIPD prototype chips (AGIPD0.2 to AGIPD0.4) is shown in figure 1. Common to all prototype chips is the preamplifier (preamp), which is a CMOS inverter with a DC gain of ~ 20 and three feedback capacitors in parallel. At the beginning of the integration only the smallest feedback capacitor is connected ($C_{f,high}$), therefore providing the highest gain and being referred to as high gain stage. The output of the preamplifier is connected to the dynamic gain switching logic, which is comparing the output voltage to an adjustable threshold voltage and is then adding a 2nd or 3rd feedback capacitor, if the signal is still exceeding the threshold value after a given amount of time. The information about the used gain stage is stored as a voltage (V_{dd} , $V_{dd}/2$, 0), which is written from the dynamic gain switching logic block to an analog storage cell array. The preamplifier stage is AC coupled to a CDS stage. In AGIPD0.4 this is realized with a selectable coupling capacitance, which allows adjusting the gain. The output of the CDS stage is stored in an

analog cell array, which is read out via the pixel buffer. Depending on the prototype version, the pixel buffer is either a voltage follower (AGIPD0.2) or an operational amplifier in charge sensitive configuration (AGIPD0.3 & AGIPD0.4), followed by a column buffer in case of AGIPD0.4. The signals are routed by a MUX (*multiplexer*) to a fully differential off-chip driver and finally digitized by an external ADC (*analog digital converter*).

The measurements of the dynamic range have been mainly carried out for AGIPD0.2 and AGIPD0.4, therefore only the major changes between these two prototype chips will be mentioned here:

- While AGIPD0.2 only features a 100 fF feedback capacitor for the high gain stage, a major change with respect to the dynamic range was the implementation of a smaller feedback capacitor of 60 fF into some rows of AGIPD0.4, in order to increase the gain in the high gain stage [5]. Common for both prototype versions is the 2nd capacitor, defining the medium gain stage, which has a size of $C_{f,med} = 3$ pF and the 3rd capacitor (low gain stage) with a capacitance of $C_{f,low} = 10$ pF.
- AGIPD0.2 has a fixed CDS gain of 2, while AGIPD0.4 features an adjustable CDS gain of either 1 or 2. For the measurements with AGIPD0.4, it is either referred to as CDS gain low (= 1) or CDS gain high (= 2).
- A major difference between AGIPD0.2 and AGIPD0.4 is the dimension of the preamplifier reset switch, which was increased from a width of $10\text{ }\mu\text{m}$ in AGIPD0.2 to $27\text{ }\mu\text{m}$ in AGIPD0.4. A reason for the step was to increase the dynamic range of the high gain stage, as the charge injection from the reset switch is used to push the working point of the preamplifier after releasing the reset.

In the AGIPD0.4 prototype chip, different kinds of pixels have been implemented (figure 4, left):

- Standard pixel: $C_{f,high} = 100$ fF, no protection circuit
- High gain pixel: $C_{f,high} = 60$ fF, no protection circuit
- Diode pixel: $C_{f,high} = 100$ fF, diode protection circuit
- NMOS pixel: $C_{f,high} = 100$ fF, NMOS protection circuit

2.2 Dynamic range

In the case of dynamic gain switching, the maximum dynamic range is given by the lowest gain and the linear ranges of preamplifier and CDS stage.

Figure 2 shows simulations of the preamplifier output voltage ($V_{out,pre}$) as a function of incoming charge for a high gain pixel ($C_{f,high} = 60$ fF) of AGIPD0.4. The three gain stages are marked red (high gain stage), green (medium gain stage) and blue (low gain stage). The black horizontal line at 870 mV is corresponding to the preamplifier output voltage, when it is in reset. The process of writing the signals into the storage cells is the following (figure 2):

All switches of the preamplifiers feedback loop are in reset, therefore the voltage over the capacitors $C_{f,high}$, $C_{f,med}$, $C_{f,low}$ is zero. The voltage at the preamplifier output is 870 mV (black line).

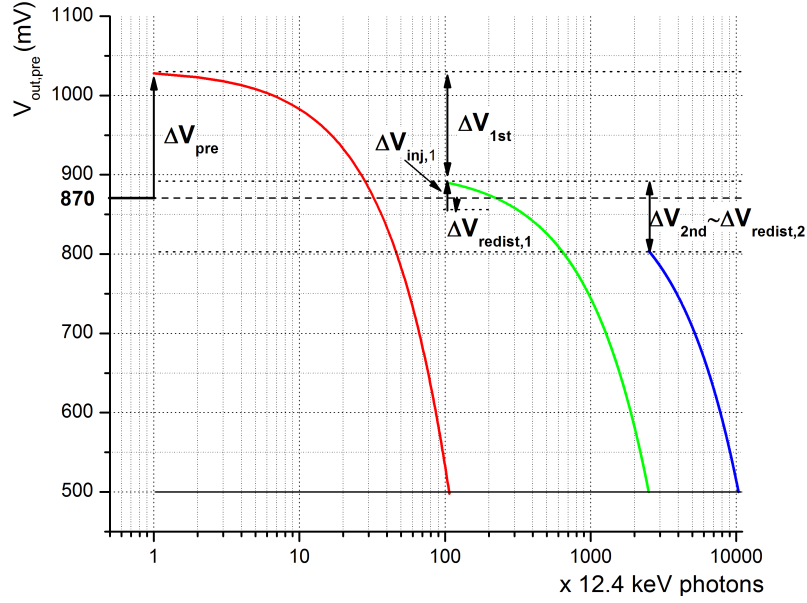


Figure 2. Simulated response of the preamplifiers output of an AGIPD0.4 pixel with a high gain pixel ($C_{f,high} = 60$ fF). (Red curve: high gain stage, green curve: medium gain stage, blue curve: low gain stage).

The preamp reset switch is released (NMOS switch), injecting the charge Q_{inj} into $C_{f,high}$ causing a voltage step of $\Delta V_{pre} = +163$ mV (eq. (2.1)) and shifting the operating point to 1033 mV. This charge injection is used to extend the dynamic range of the high gain stage by $25 \cdot 12.4$ keV photons.

$$\Delta V_{pre} = \frac{Q_{inj}}{C_{f,high}} \quad (2.1)$$

A swing at the preamp output of 533 mV with a non-linearity less than 1% can be expected, when setting the gain switching threshold at $V_{th} = 500$ mV. With a simulated gain of $m_{high} = 6.50$ mV/12.4 keV, 533 mV correspond to a dynamic range in the high gain stage of $107 \cdot 12.4$ keV photons.

When the preamplifier output voltage is exceeding the threshold voltage, a 2nd feedback capacitor ($C_{f,med} = 3$ pF) is added into the feedback loop. Adding this capacitor is causing two voltage steps:

1. $\Delta V_{inj,1}$: charge injection into $C_{f,med}$ and $C_{f,high}$ from the switch connecting $C_{f,med}$ (transmission gate, $\Delta V_{inj,1} = +29$ mV)
2. $\Delta V_{redist,1}$: charge redistribution from $C_{f,high}$ into $C_{f,med}$ and $C_{f,high}$.

With an estimated parasitic capacitance of $C_p = 33$ fF in the feedback loop and ΔV_{high} being the voltage across $C_{f,high}$ with respect to the reset voltage, the operating point due to charge redistribution shifts by $\Delta V_{redist,1} = -10$ mV or 3.0% of ΔV_{high} , according to eq. (2.2). The voltage step due to charge redistribution is defined by the ratio of the capacitances before and after gain switching:

$$\frac{\Delta V_{redist,1}}{\Delta V_{high}} = \frac{C_{f,high} + C_p}{C_{f,high} + C_{med} + C_p} \approx 3.0\% \quad (2.2)$$

Overall, the operating point after the first gain switching changes according to eq. (2.3):

$$\Delta V_{1st} = \Delta V_{pre} + \Delta V_{inj,1} + \Delta V_{redist,1} \quad (2.3)$$

The operating point after the first gain switching shifts by $\Delta V_{1st} = -144$ mV with respect to the start of the integration to an absolute value of 889 mV. ΔV_{1st} is strongly dominated by the initial charge injection into $C_{f,high}$ causing ΔV_{pre} .

If the signal at the preamplifier output still exceeds the threshold voltage after a given amount of time after the 1st gain switching, a 3rd capacitance $C_{f,low} = 10$ pF is added into the feedback loop. As in case of the 1st gain switching, there will be two voltage steps:

1. $\Delta V_{inj,2}$: charge injection from releasing the $C_{f,low}$ switch into $C_{f,low}$, $C_{f,med}$, $C_{f,high}$ (NMOS switch, $\Delta V_{inj,2} = +2$ mV).
2. $\Delta V_{redist,2}$: charge redistribution from $C_{f,med}$ and $C_{f,high}$ into $C_{f,low}$, $C_{f,med}$, $C_{f,high}$.

Taking into account the parasitic capacitance, the shift of the operating point is given by eq. (2.4). The voltage step due to the redistribution of charge is given by ratio of feedback capacitors and the voltage swing of the medium gain stage with respect to the reset voltage ($\Delta V_{med} = 370$ mV), resulting in a voltage step of 23.6% of ΔV_{med} or $\Delta V_{redist,2} = -87$ mV.

$$\frac{\Delta V_{redist,2}}{\Delta V_{med}} = \frac{C_{f,high} + C_{f,med} + C_p}{C_{f,high} + C_{med} + C_{f,low} + C_p} \approx 23.6\% \quad (2.4)$$

Overall, the voltage step at the 2nd gain switching point is given by eq. (2.5) and is $\Delta V_{2nd} = -85$ mV:

$$\Delta V_{2nd} = \Delta V_{inj,2} + \Delta V_{redist,2} \quad (2.5)$$

Comparing the contributions of the voltage step ΔV_{2nd} , the input from the charge injection by operating the $C_{f,low}$ switch (NMOS switch) is negligible due to the relatively big capacitance the charge is injected into and the voltage step is dominated by charge redistributed into $C_{f,low}$.

Overall, the voltage step at the 1st gain switching point (ΔV_{1st}) is mainly arising from an intended precharging of $C_{f,high}$, in order to increase the dynamic range in the high gain stage. The 2nd voltage step (ΔV_{2nd}) is dominated by charge redistribution. Each voltage step is reducing the overall achievable dynamic range of the ASIC, as it is consuming part of the linear dynamic range of the preamplifier and/or CDS stage. Therefore, the implementation of a dedicated precharging scheme of the feedback capacitors will be investigated to make use of the whole dynamic range.

As summary the expected gain switching points of AGIPD0.4 for the high gain pixel ($C_{f,high} = 60$ fF) have been calculated, taking into account the results from the simulation:

- 1st switching point: $107 \cdot 12.4$ keV
- 2nd switching point: $2505 \cdot 12.4$ keV photons
- The overall dynamic range will exceed $1 \cdot 10^4 \cdot 12.4$ keV

The Poisson limit at the 1st switching points is $10.3 \cdot 12.4$ keV photons and $50.0 \cdot 12.4$ keV photons at the 2nd switching point. As reported before [5], the noise performance of AGIPD0.4 ($C_{f,\text{high}} = 60$ fF) is $300 e^-$ ENC or less than $0.1 \cdot 12.4$ keV photons. The noise performance in the other gain stages was measured to be around $4.5 \cdot 12.4$ keV photons in the medium gain stage and around $30 \cdot 12.4$ keV photons in the low gain stage. Therefore, according to the calculations, the noise performance should be better than the Poisson limit for the whole dynamic range.

2.3 Protection circuits

In order to protect the input of the preamplifier against high voltage input swings, as it happens in case of high intensity spots, several protection circuits have been investigated (figure 4, left). Two different kinds of protection circuits have been investigated: a diode structure and a NMOS structure in diode configuration. Both are connected to an adjustable voltage at their backside, here referred to as V_{prot} . This voltage defines the threshold at which the protection circuit starts to remove charge from the input of the preamplifier.

2.4 Measurement setup

The aluminum backside contact of the AGIPD sensors has been etched away to allow the injection of light into the sensor. The measurements have been performed with an infrared laser setup using a laser diode from PicoQuant (LDH-P-F-1030) with a wavelength of 1030 nm. The pulsed laser diode is controlled by a base unit which is triggered by the AGIPD test setup. If not triggered, the laser can be operated in burst mode at a repetition rate between 5 MHz to 80 MHz. The delay between triggering and the release of the laser shot is ~ 35 ns and the pulse duration is around 5 ps. The laser intensity can be varied continuously using a potentiometer (< 15 mW) or by means of two filter wheels with 6 neutral filters each, allowing for 36 combinations. The laser beam is fed into the filter wheels with a 5-axis goniometer unit. Behind the filter wheel, there is a beam expander to widen the beam, followed by an iris and a focusing lens with 20 mm focal length. The laser setup allows for the creation of an adjustable number of electron-hole pairs in the sensor at a rate of 5 MHz, which is comparable to the rate of incoming photon pulses at the European XFEL.

Pixels were illuminated with the infrared laser (1030 nm) at full power corresponding to roughly $2 \cdot 10^5 \cdot 12.4$ keV photons. The laser emitted single pulses, being activated by an external trigger, when the chip was integrating charge. The focus size on the sensor surface was less than $10 \mu\text{m}$.

Another option, which allows a closer investigation of the dynamic range is using a bulb in connection with a large capacity battery. This setup generates electron-hole pairs at a very constant rate, allowing to precisely step the dynamic range by varying the integration time. However, as the electron-hole pairs are created continuously, their temporal creation is very different with respect to an XFEL. Moreover, as the integration time is increased, more shot noise from the sensor is introduced. On the other hand, noise measurements with the laser diode revealed shot-to-shot fluctuations of around 5%. This is typically much worse than the noise performance of the detector and therefore not usable, especially for noise measurements at high laser intensities.

A cross calibration is possible by performing an energy calibration measurements with an X-ray tube, using fluorescence radiation from germanium (Ge), molybdenum (Mo), silver (Ag) and

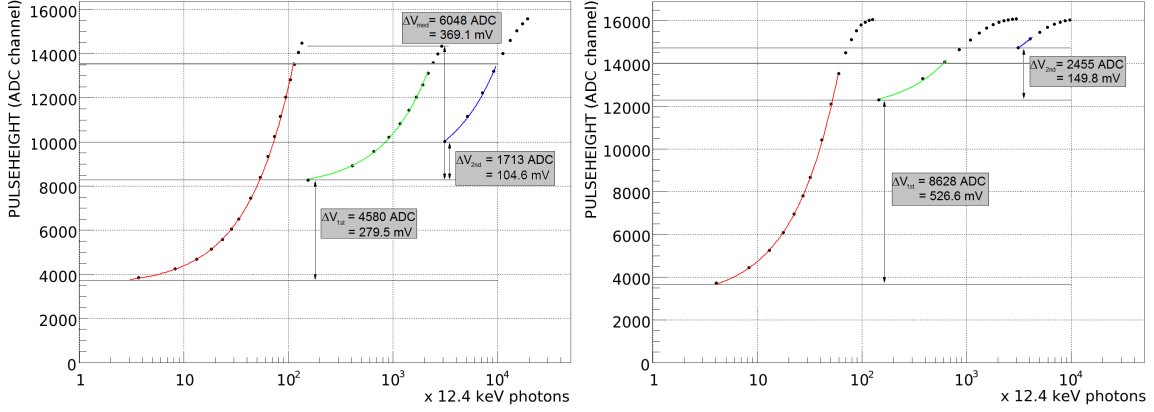


Figure 3. Measured dynamic gain switching of AGIPD0.4 with $C_{f,\text{high}} = 60$ fF and CDS gain of 1 (left) and a CDS gain of 2 (right). The high gain stage is marked in red, the medium gain stage is green, the low gain stage is blue.

tin (Sn). A cross calibration can be performed for all three gain stages by performing linear fits for the other gain stages and taking the gain ratios with respect to the high gain stage.

3 Results

3.1 Dynamic range

The measurements of the dynamic range have been carried out by using the illumination with a light bulb connected to a battery. Figure 3 shows the dynamic range of AGIPD0.4 with $C_{f,\text{high}} = 60$ fF with a CDS gain of 1 (left) and 2 (right).

In the case of a CDS gain of 1, a maximum dynamic range of around to $1 \cdot 10^4 \cdot 12.4$ keV photons could be measured. Due to the low gain of the CDS stage the noise of the high gain stage is around $553 e^-$ ENC or $0.16 \cdot 12.4$ keV photons. The noise in the medium gain stage is roughly $7.8 \cdot 12.4$ keV photons and $45 \cdot 12.4$ keV photons in the low gain stage. The gain switching point between high and medium gain stage is at $110 \cdot 12.4$ keV photons, having a noise performance better than the Poisson limit ($10.5 \cdot 12.4$ keV photons) at the gain switching point. The gain switching point between medium and low gain stage lies at around $3200 \cdot 12.4$ keV photons. The electronic noise at the gain switching point ($45 \cdot 12.4$ keV photons) is again better than the Poisson limit ($57 \cdot 12.4$ keV photons).

The noise performance improves using a CDS gain of 2. The noise of the high gain stage is around $300 e^-$ ENC or $0.1 \cdot 12.4$ keV photons. The noise performances of the medium and low gain stage are around $4.5 \cdot 12.4$ keV photons and $30 \cdot 12.4$ keV photons, respectively. As the points of gain switching are not influenced by a higher CDS gain, the noise at the switching points is well below the Poisson limit. However, in this configuration the dynamic range with a non-linearity better than 1% (rms) reaches only up to about $600 \cdot 12.4$ keV photons.

One reason for the reduced dynamic range is the limited linear range of the CDS stage. In order to cover the dynamic range possibly provided by the preamplifier, the CDS stage needs to cover a voltage swing of around 1066 mV. However, according to simulations only about 500 mV are available.

Another reason for that behavior is the reduction of $C_{f,\text{high}}$ from 100 fF to 60 fF without rescaling the preamp reset switch. Therefore, the charge injection from the reset switch causes a much higher precharging of $C_{f,\text{high}}$ defining the operating point of the preamplifier. As the CDS stage defines the sampling point, most of the overall dynamic range provided by the CDS stage is consumed by the high gain stage before entering saturation for the medium and especially the low gain stage, making the low gain stage virtually not usable.

For comparison with the simulations, measurements with a CDS gain of 1 were taken into account, where preamplifier and CDS stage were operating in their linear regime.

Simulations indicate that the voltage step after switching to the low gain stage (2nd voltage step) is dominated by the charge redistribution into the low feedback capacitor, which will be around 23.6% of the voltage swing of the medium gain stage according to eq. (2.4).

Measurements reveal a voltage swing of the medium gain stage of 6048 ADC units, corresponding to 369 mV (1 ADU = 61.0 μ V) (figure 3, left). The voltage step after switching to the low gain stage is 28.3% of the medium gain stage voltage swing. Part of the voltage swing happened within the non-linear region of the CDS stage (non-linearity > 1%, marked by the grey line at 13500 ADC units), underestimating the actual voltage swing. Together with the error in determining the exact position of gain switching, that explains the deviation from measurement and simulation of 4.7%.

From the measurements a ratio between 1st and 2nd voltage step ($\Delta V_{1\text{st}}/\Delta V_{2\text{nd}}$) of 2.67 can be calculated, compared to a value of 1.69 extracted from simulations. As the values of $\Delta V_{2\text{nd}}$ from measurement and simulation are in good agreement, $\Delta V_{1\text{st}}$ (dominated by the charge injection from the preamplifier reset switch) is underestimated in the simulation by roughly 37%.

The voltage step height $\Delta V_{1\text{st}}$ changes, when changing the CDS gain from low (= 1) from 4580 ADC units (= 279.5 mV) to 8628 ADC units (= 526.6 mV) for the high CDS gain (= 2) (figure 3). The ratio of the steps is 1.88, corresponding to the increase of the CDS gain, thus indicating that the step originates from the preamplifier stage. In AGIPD0.4, the preamplifier reset switch, which is defining ΔV_{pre} and dominating the voltage step height between high and medium gain stage, has a width of 27 μ m. In AGIPD0.2 the reset switch has a width of 10 μ m. The voltage steps $\Delta V_{1\text{st}}$ of AGIPD0.4 pixels and AGIPD0.2 pixels with the same properties ($C_{f,\text{high}} = 100$ fF, CDS gain of 2) are 6000 ADC units (= 366.2 mV) (AGIPD0.4) and 2000 ADC units (= 122.1 mV) (AGIPD0.2), respectively. Therefore, the voltage step height in AGIPD0.4 is 3 \times higher than in AGIPD0.2, which scales with the ratio of the preamplifier reset switches ($\times 2.7$). These findings confirm the expectation that the charge injection from the preamp reset switch is dominating the 1st voltage step and that this step is correlated to the size of the reset switch.

Therefore, it is planned to change the width of the reset transistor to 5 μ m in an upcoming submission, reducing the dynamic range of the high gain stage from 533 mV to 350 mV. According to these numbers a new CDS buffer has been designed, being able to provide a good linearity from 600 mV to 1350 mV, thus being able to cover the whole dynamic range of the preamplifier with a CDS gain of 2. In this case, the gain switching points were calculated to be at around $70 \cdot 12.4$ keV photons (high to medium) and $2700 \cdot 12.4$ keV photons (medium to low). The low gain stage should be able to reach at least to $1 \cdot 10^4 \cdot 12.4$ keV photons with a non-linearity of less than 1% (rms).

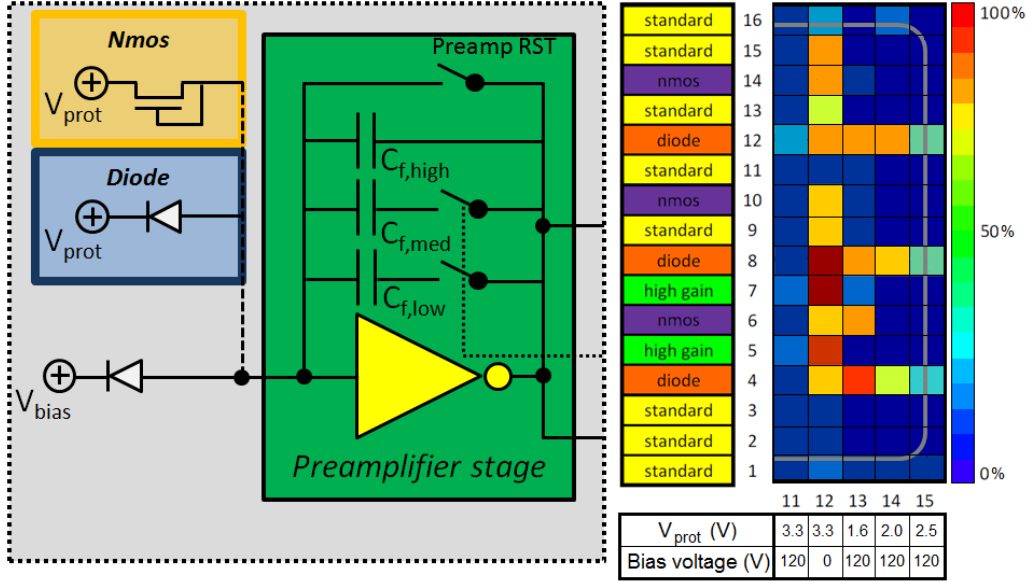


Figure 4. (Left) Protection circuits against high voltage swings at the input of the preamplifier. (Right) Distribution of the pixel output of a part of the pixel matrix (columns 11 to 16) after the measurement of the protection circuits using the infrared laser diode. The different pixel variations in AGIPD0.4 are implemented along the different rows, as indicated on the left side. The voltage at the backside of the protection circuit V_{prot} and the sensor high voltage V_{sensor} were varied column-wise during the laser testing, as given in the table below the pixel output map. The color map assigns low step heights to blue colors and high step heights to red colors. The dead pixels in column 12 are due to user misoperation. The reduced step height of the diode protected pixels in column 15 arises from a partial shielding of the pixel by the aluminum backside contact (marked in gray).

3.2 Protection circuits

The input protection circuits of the preamplifier were tested by illuminating single pixels with an infrared laser, in order to simulate a charge pulse at the preamplifier input, which corresponds to a pulse created by $2 \cdot 10^5 \cdot 12.4 \text{ keV}$ photons. The center of each pixel was illuminated with the aforementioned laser properties for approximately 1 sec in triggered mode (5 MHz). During the test, various parameters were varied column-wise:

- The protection voltage V_{prot} was varied between 1.6 V and 3.3 V
- The sensor bias voltage V_{sensor} was either set to +120 V or 0 V

After the test, the chip was homogenously illuminated with visible light from a bulb and the pixel outputs were measured (figure 4, right). The table below the pixel map in figure 4 is showing the operation parameter during the laser test. The color coding of the pixels is corresponding to the pixel output, from blue (no signal) to red (high signal). The reduced signal of the diodes at column 15 (light green) is due to partial shielding of light entering the sensor because of the aluminium backside contact (the aluminium edge is marked by the grey line). Different conclusions can be drawn from the results in figure 4 (right), which are summarized in table 1:

Table 1. Relative number of surviving pixels after the protection circuit measurements. The number in brackets gives the number of investigated pixels.

V_{prot} (V)	No protection	Diode	NMOS switch
1.6	0% (8)	100% (3)	33% (3)
2.0	0% (8)	100% (3)	0% (3)
2.5	0% (8)	100% (3)	0% (3)
3.3	0% (8)	0% (3)	0% (3)

1. Pixels without protection circuit (rows: 1, 2, 3, 5, 7, 9, 11, 13, 15, 16) are not responding to illumination after testing with the laser.
2. Pixels with a NMOS switch as protection circuit (rows: 6, 10, 14) are not functional anymore after the laser testing. (Except one single pixel with $V_{\text{prot}} = 1.6$ V (column: 13).
3. Pixels with a protection diode (rows: 4, 8, 12) are functional after testing with the laser up to a protection voltage V_{prot} of 2.5 V (columns: 13, 14, 15). After increasing V_{prot} to 3.3 V, no pixel was working anymore after probing with the laser (column: 11).
4. When the sensor bias voltage was switch off ($V_{\text{sensor}} = 0$ V) during the laser probing, all pixels showed a response in the following test with visible light of the bulb (column: 12). (Single destroyed pixels in between are due to user misoperation.)
5. When the sensor bias voltage V_{sensor} of +120 V was applied to the sensor backside during the laser testing (column: 11), all pixels were destroyed and showed no signal in the test with the light bulb. This could indicate that the actual process of destroying the pixel could be the creation of a conductive channel in the sensor. This would cause the sensor bias voltage be applied to the preamplifier input, exceeding its breakdown voltage.

Measurements of the noise show no difference in the noise performance of the pixels, indicating that the protection circuits are not significantly adding capacitance to the input of the preamplifier. Moreover, no significant charge leaking through the diode could be measured in case of high input charges.

4 Conclusions

AGIPD0.4 prototype chips have been extensively characterized in preparation of the submission of the first full scale chip AGIPD1.0.

Measurements of the dynamic range showed that AGIPD0.4 will not be able to cover the requested dynamic range of at least $10^4 \cdot 12.4$ keV photons and ensure single photon resolution in the high gain stage. Several design optimizations are proposed, such as improving the range of the CDS stage and reducing the preamplifiers reset switch size to increase the limited dynamic range of AGIPD0.4 (60 fF, CDS gain of 2). The calculated dynamic range of AGIPD1.0, implementing a smaller preamp reset switch ($W = 5 \mu\text{m}$) and employing an improved CDS stage, will be exceeding

the requested dynamic range of $1 \cdot 10^4 \cdot 12.4 \text{ keV}$ photons, while keeping single photon resolution in the high gain stage.

Moreover, protection circuits at the input of the preamplifier were investigated. Test measurements with an IR laser revealed that protection diodes with a reference voltage of 2.5 V provide a good protection of the pixel inputs. These pixels showed a noise performance which was very similar to non-protected pixels. No leaking could be observed for high input signals.

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