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The PERCIVAL soft X-ray imager

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ABSTRACT: With the increased brilliance of state-of-the-art Synchrotron radiation sources and the advent of Free Electron Lasers enabling revolutionary science with EUV to X-ray photons comes an urgent need for suitable photon imaging detectors. Requirements include high frame rates, very large dynamic range, single-photon counting capability with low probability of false positives, and (multi)-megapixels.

PERCIVAL ("Pixelated Energy Resolving CMOS Imager, Versatile and Large") is currently being developed by a collaboration of DESY, RAL, Elettra and DLS to address this need for the soft X-ray regime. PERCIVAL is a monolithic active pixel sensor (MAPS), i.e. based on CMOS technology. It will be back-thinned to access its primary energy range of 250 eV to 1 keV with target efficiencies above 90%. According to its preliminary specifications, the roughly $10 \times 10\,\mathrm{cm}^2$, 3520×3710 pixel monolithic sensor will operate at frame rates up to 120 Hz (commensurate with most FELs) and use multiple gains within its $27\,\mu$m pixels to measure (e.g. at 500 eV) 1 to $\sim 10^5$ simultaneously-arriving photons.

Currently, small-scale front-illuminated prototype systems (160×210 pixels) are undergoing detailed testing with visible-light as well as X-ray photons.

KEYWORDS: imager; soft X-ray; CMOS; MAPS; FEL; synchrotron; camera.

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Contents

1. Introduction

With the increased brilliance of state-of-the-art Synchrotron radiation sources and the advent of Free Electron Lasers enabling revolutionary science with EUV to X-ray photons comes an urgent need for suitable photon imaging detectors.

FEL experiments are often designed accepting the destruction of the sample by a single pulse, making the recording of shot-by-shot frames as individual images a necessity in many cases. Thus FELs require imaging detectors running at the FEL's pulse repetition rate. For most of today's FELs, this rate is in the tens to hundred Hz (120 Hz at LCLS).

With on the order of 10^{13} and more photons impinging on a sample in a single FEL pulse, e.g. individual bragg spots from nanocrystals can easily encompass 10^5 or even 10^6 photons in a single image. Conversely, weaker signatures (e.g. at larger diffraction angles, or from weaker-diffracting samples) are made up of few or even single photons. Thus an optimized imager for FEL applications must be able to reliably handle a large dynamic range (ideally 1 – 10^5 photons or more), and even-brighter diffraction signatures should not impede image quality in adjacent pixels.

With a single FEL pulse as short as tens of femtoseconds, and much more than only one photon arriving in a pixel during such a short time period, obviously an integrating (rather than photon-counting) pixel design is required.

In order to record a large range of diffraction angles, at good angular resolution, imagers with at least on the order of $1\text{k} \times 1\text{k}$ pixels (more is better) and moderate pixel sizes (tens of μm) are needed. While data are recorded in angular space, and thus in principle a larger-pixel detector would only have to be positioned further from the interaction point, practical limitations e.g. of vacuum vessel and hutch sizes demand pixel sizes in the 10 – 100 μm range. Since gaps in the detector's imaging area significantly increase ambiguities in sample reconstruction, gapless or small-gap imaging areas are preferred.

For weakly-diffracting samples for which the per-pulse diffraction signal consists only of a handful of photons in total, the most critical property of an imaging detector is its single-photon counting capability, *combined with a very low probability of reporting false positives*. If no more than one pixel in a 1M pixel imager may falsely report a photon due to noise — not an unrealistic requirement if e.g. no more than 20 signal photons are expected — this implies a maximum allowable false positive rate per pixel per image of 10^{-6}, or a detection threshold of $\sim 4.7\sigma$ in case of gaussian noise. Of course, especially for such low-diffraction samples an as-high-as-possible quantum efficiency of the imaging system is highly desirable as well. Since bragg peaks can be sub-pixel size, the quantum efficiency should also be approximately uniform over each pixel.

Since a camera system even approximately fulfilling the needs described above was not available for the soft X-ray regime (for our purposes: 250 eV to 1 keV), in 2011 we started developing a dedicated soft X-ray imager: PERCIVAL.

2. The PERCIVAL sensor

CMOS sensors offer several advantages over other detection approaches for the described needs. They can generally be faster than CCDs as their architectures lend themselves to massive parallelization, enabling high speed at low noise; moreover, in-pixel intelligence can be integrated. Compared to hybrid pixel detectors, smaller photodiode capacitances can be realized in a monolithic CMOS imager, again enabling lower noise. In addition, small pitches of few tens of μm are less problematic in CMOS imagers since there is no need to push the boundaries of bump bonding technology, and the monolithic design also reduces complexity. Conversely, while at higher photon energies above few keV CMOS sensors are at a disadvantage due to the relatively thin commercially available epilayers (10s of μm), this active detection layer is thick enough for photons in the soft X-ray regime of PERCIVAL.

Several key needs for the PERCIVAL sensor were already discussed above (see section 1): single-photon sensitivity with low probability of false positives in combination with large dynamic range and uniformly high quantum efficiency in the 250 eV to 1 keV regime, operation up to 120 Hz, pixel size in the 10 – 100 μm range, and Megapixel or larger sensor. The need for a low probability of false positives even at 250-300 eV converts to a need for a noise level (best significantly) below 15 e^- rms. To minimize noise, even at the relatively short integration times needed the operating temperature must be kept at around -30°C – -40°C. The dynamic range needed (reliable single photon detection to 10^5 photons) would imply a brute-force digitization dynamic range of better than $\sim 10^6$ or 20 bit; instead multiple gains (4 gain levels) are implemented.

In addition to these key needs, a cloverleaf arrangement with central hole must be possible to arrange sensors around the path of the undiffracted beam or cover a larger area. In order to allow this, the sensors should be buttable at two adjacent edges.

Given the emphatic desire in the community for large sensor areas without butting edges, a single PERCIVAL sensor will have an active imaging area of $\sim 10 \times 10\,\mathrm{cm}^2$, comprising 3520×3710 pixels of 27.0 μm pitch. This is slightly larger than the 25 μm pitch of the current test sensor, the change was made to optimize "full well capacity" per unit area of the full sensor.

One key challenge is the desire to achieve high quantum efficiency in the soft X-ray regime down to $\sim$250 eV. At this energy, attenuation lengths in both Si and SiO_2 are on the order of 0.1 μm,

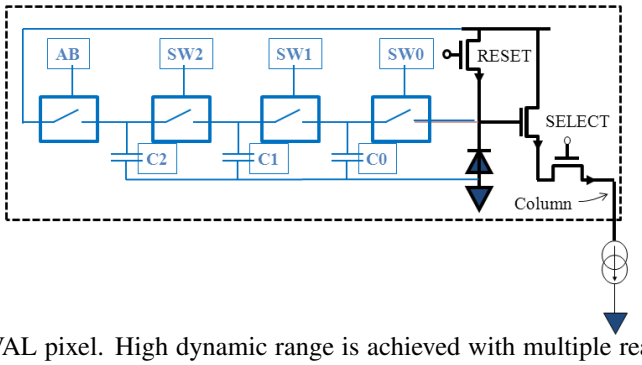

Figure 1. The PERCIVAL pixel. High dynamic range is achieved with multiple readings and lateral overflow. In black the basic 3T pixel, in blue the added overflow structure.

and thus passive entrance windows of few, certainly no more than tens of, nm are required to enable quantum efficiencies above ∼90%. This makes backthinning and back-illumination indispensable, and special care must be taken to reduce the entrance window thickness.

The PERCIVAL sensor is being designed by RAL/STFC. A block diagram of the full sensor is shown in figure 2. Figure 1 illustrates the pixel architecture: The basic 3T structure (source follower, reset, and select transistors) is enhanced by the addition of a series of switches (SW0-2, AB) and capacitors (C0-C2). During charge integration, the gates of the SW transistors connecting the capacitors are biased moderately at around 0.7V. Under low-flux conditions, the diode voltage is not lowered much from its reset voltage (around 2V), no current can flow through the transistors to the capacitors, and the system behaves like an ordinary 3-Transistor Active Pixel Sensor. At higher photon fluxes, the diode voltage is lowered significantly, to to the point where the diode voltage becomes comparable to the transistor gate voltage. At this point, subthreshold current will start flowing, starting charging the (first) additional capacitor, while the voltage on the diode will stay roughly constant — the system has switched to its second-highest gain mode by combining the capacitance of the diode and the C0 capacitor. During readout, the switches SW0-2 are sequentially opened (resulting in ever increasing effective pixel capacitance) and the resulting source-follower voltages are compared to a threshold in the sampling stage to identify which of the four overall capacitances (and thus gains) is best suited to the charge recorded within the particular pixel and image. In normal operation, only this "best" voltage is passed on to the ADC for conversion (and the gain information is stored).

The ADC consists of a coarse and fine stage with two different current ramps, allowing for a total of 12-bit (plus one bit overrange) conversion. Together with the 2-bit information recording the gain (= SWx switch setting), 15 bits per pixel and reading must be transmitted to the readout. The sensor is designed to allow for digital correlated double sampling (CDS), i.e. recording the baseline voltage in each pixel before charge integration, and this information — although useful only for the highest gain based on diode capacitance only — is also converted into the same 15 bits.

In order to achieve readout rates of 120 Hz over 3710 rows, 7 ADCs per column operating at 7 μs conversion time are used. Data from 32 columns is multiplexed into one LVDS data output line running at ∼460 MHz data rate. In total, 111 LVDS lines output the data from 24864 ADCs, resulting in 50 Gbit/s (including CDS) image data from a single sensor running at 120 Hz.

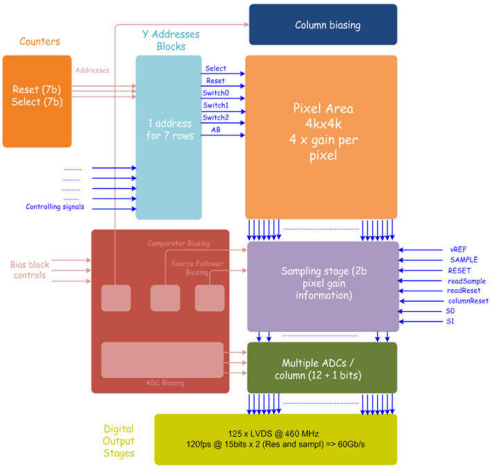

Figure 2. The PERCIVAL full sensor block diagram.

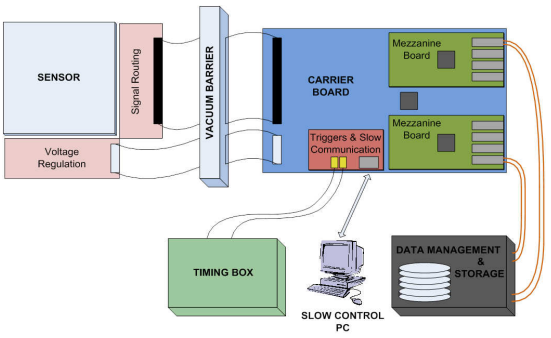

Figure 3. Block diagram of the PERCIVAL camera.

3. The PERCIVAL camera system

The PERCIVAL camera will consist of the CMOS sensor itself plus a combination of electronics boards for power supply, bias, control, and readout – in addition to the mechanical infrastructure required to keep sensor and electronics at optimum operating temperatures, and the computing infrastructure to handle the 50 Gbit/s continuous data stream.

Figure 3 shows a block diagram of the camera system. Critical bias and supply voltages will be generated in vaccum close to the sensor on a "Periphery Board". It is intended to use Low-Temperature Cofired Ceramics (LTCC) here due to its good thermal-expansion match to Si. The choice of LTCC as PCB material will likely entail splitting this into two physically separate PCBs, with both performing a mix of signal distribution and voltage regulation. This in-vacuum board will also host monitoring capabilities for biases as well as temperatures. From the Periphery board, input ($\sim$100) and output ($\sim$120) LVDS lines will have to be routed through flexible leads of several 10s of cm and a vacuum flange to the outside of the chamber, where they connect to a "Carrier" board. This Carrier board will host an FPGA running the finite state machine (FSM), a "Trigger & slow communication" board for receiving timing and control inputs from the outside world, and two "Mezzanine" boards each hosting one FPGA for data handling, memory, and four 1-10Gbit ethernet links. This Mezzanine board [1] is a custom DESY development shared by AGIPD [2, 3], LAMBDA [4], and PERCIVAL, and is already used in todays test configuration.

While the sensor functions at room temperature, optimized noise performance is expected around -40°C, and many science applications demand that the sensor be mounted movable within the vacuum chamber. The mechanics, cooling approach, and physical layout of the electronics for the full-size sensor will be designed with maximum user flexibility in mind.

4. The PERCIVAL test system

Test chip(s) Before designing and fabricating a full $10 \times 10\,\mathrm{cm}^2$ chip, smaller test sensors were produced to both evaluate the performance of various pixel architectures, gain decision logic, and

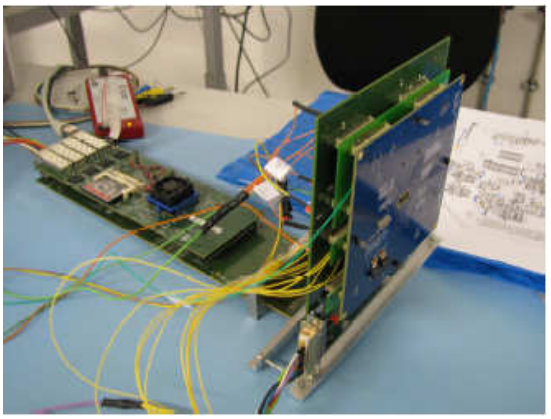

Figure 4. The test setup on a benchtop. From right to left, CoB with test chip, interposer board, periphery board. The latter connects to the horizontal SD board (note the vacuum barrier flange already in place), on which in turn the Mezzanine board is placed. See text for details.

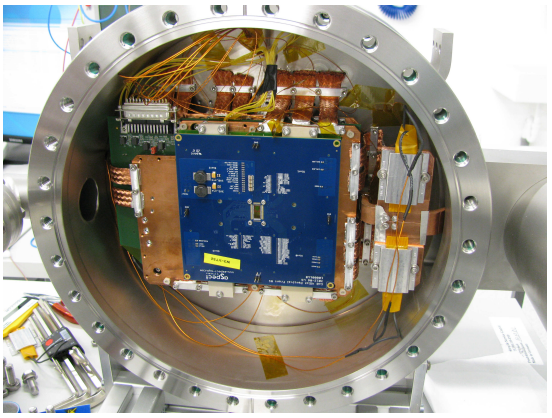

Figure 5. The open PERCIVAL test chamber. Copper plates thermally tied to the chamber surround the Periphery board and provide cooling paths to hot active components, tied to the chamber walls. The cryocooler sits in the chamber extension to the right, resistors on the cold finger provide counter-heating.

the ADC and to verify the fast digital output circuitry. The sensors are fabricated in a commercial 180nm CMOS technology.

Test Sensors 1 and 2 ("TS1" and "TS2"), with 210×160 25-μm-pixels each, allow comparison of a total of 12 different pixel designs (70×80 pixels each), with identical periphery. Half use an annular partially pinned photodiode [5], half are based on a more conventional n-well diode design. These sensors use slower CMOS output lines (8 single-ended CMOS outputs nominally running at 20 MHz) and slightly less efficient data formatting (12% padding zeroes), but enable testing of the pixel and ADC performance at full readout and conversion speeds. TS1 and TS2 are currently undergoing detailed testing in front-illuminated configuration (see section 5). After preliminary tests ascertained TS1 and TS2 are functioning properly, wafers with TS1 and TS2 chips on 18 μm epilayer were forwarded to NASA's Jet Propulsion Laboratory (JPL) for backthinning; first backthinned TS1 and TS2 chips are expected in January 2014. The TS1 and TS2 chips are wire-bonded to a carrier board (Chip on Board, or CoB) which interfaces to both the custom readout system described in section 4 and the standard imager test system employed at RAL/STFC.

A separate test sensor, "TS3", encorporates the more efficient multiplexing and faster data streamout needed for the full sensor. Data from 32 columns with their 7 (+ one backup) ADC are multiplexed to a single LVDS output. TS3 also incorporates a PLL, on-chip bias current generation, and LVDS inputs. At room temperature, the TS3 performs as expected, tests at operating temperature (around -40°C) are expected to yield similar results.

Readout The readout system designed by the collaboration for the PERCIVAL test chips was planned in order to enable testing the performance of the in-vacuum periphery board circuitry. Figure 4 shows the assembled electronic components on a benchtop. The CoB board is connected to an interposer board – this became necessary to allow added test access and enable some fixes and improvements of the first periphery board – which in turn is connected to the "Periphery board".

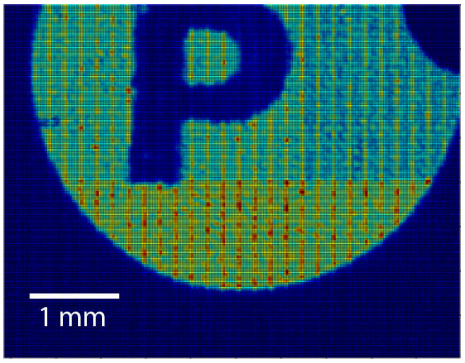

Figure 6. Shadowgram of a laser-printed "P" on overhead foil, illuminated with a white-light LED and recorded by a front-illuminated PERCIVAL TS2 chip. Note that differences in row metallization, with a 7-row periodicity (top-to-bottom in the image), are apparent, as are the boundaries of the sectors with different pixel types.

This in-vacuum board provides all supply and bias voltages and (for the test system) bias currents, all programmable. Diagnostics for the provided currents and voltages as well as temperature are available. For the test chip, CMOS↔LVDS conversions on ∼100 lines are also required and are performed here. The periphery board is powered from a stack of commercial low-voltage power supplies. Its data lines plug into a compact 500-pin connector on a signal distribution ("SD") board borrowed from the LAMBDA [4] project. This board is also designed to allow integration with a custom vacuum flange. On the air side of the SD board, one "Mezzanine" board provides the FPGA needed for the finite state machine (FSM) commanding of the chip as well as data handling, memory, and four 1-10Gbit ethernet links. The test system has been integrated into a vacuum vessel with a Cryotiger cooling system to easily achieve and compare performances at operating temperatures down to ∼-40°C, and enable soft X-ray testing. Figure 5 shows the open test chamber.

5. First photons

The PERCIVAL TS1/2 test chips, in front-illuminated configuration, saw first (visible) light in December 2012. Note that for both visible and (soft) X-ray illumination, front-illumination of the test sensor implies that sensor circuitry, metallization, and SiO_2 obscure the sensitive epilayer, resulting in various non-uniformities as well as overall lower QE. Figure 6 shows the shadowgram of a "P" laser-printed onto an overhead foil and mounted on a opaque carrier placed ∼1 cm in front of the sensor; the illumination is done with a simple white-light LED.

Front-illuminated PERCIVAL test sensors (one each of TS1 and TS2) were exposed to X-rays in the 300 eV – 2 keV range at Petra III's P04 soft X-ray beamline [6] in May 2013. Figure 7 shows the result of exposing a PERCIVAL TS2 chip to the direct beam at P04, at a beam energy of 2 keV and with the beam parameters tuned to give an overall beam intensity on the order of $2{\cdot}10^{10}$ ph/s. A razor blade (Figure 9) was inserted ∼17 cm before the sensor (distance given by various external constraints in this first X-ray exposure) in the photon path to provide a clear structure to image. It must be noted that the "streaking" in the image to the right of the main beam profile is due to an upstream reflection of the beam, not a detector artefact. Also, the intercalibration of ADC units from fine and coarse ramp is preliminary, and the intercalibration of gain and ADU

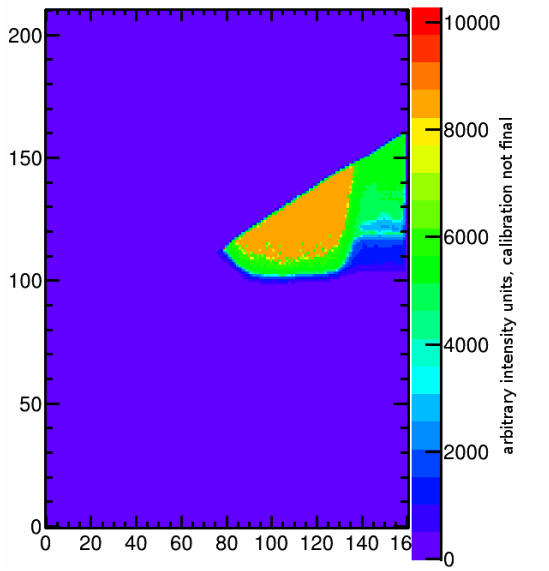

Figure 7. Dark-subtracted image of P04's (somewhat collimated) direct beam, with a $\sim$45° rotated razor blade placed in the beam's path. The streak to the right is due to upstream scattering; for details see text.

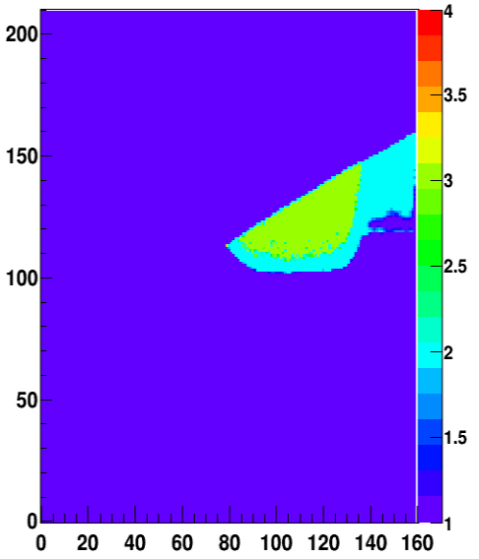

Figure 8. Gain bit only for the same P04 razor blade image, illustrating the automated pixel-by-pixel change of gain as the image intensity increases.

Figure 9. Photograph of the razor blade, here with an Al foil attenuator not used for the image above, on the manipulator arm.

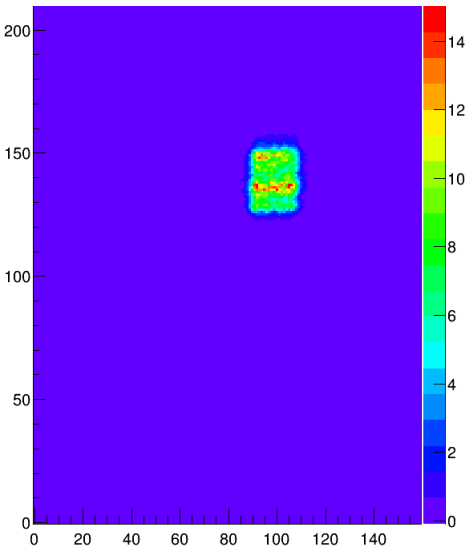

Figure 10. Dark-subtracted image of P04's direct beam, after passage through collimators and $\sim$13μm of Al foil filter, in units of 907 eV photons. For details see text.

units, affecting the numerical value of regions where lower gains are applied, are very rough first estimates only. While Figure 7 shows the full dark-subtracted image, obtained by averaging of a series of frames recorded, Figure 8 shows the gain information only, clearly illustrating that automated gain switching occurs, and is dependent on beam intensity.

Figure 10 shows the image recorded by a PERCIVAL TS1 chip of a more collimated P04 beam at 907 eV through an Al filter ($\sim$13μm kitchen Al foil). The full beam's intensity is $\sim 5 \cdot 10^{11}$ ph/s.

Using a (rough) calibration of $\sim$16.7 e^-/(preliminary ADU), the recorded per-pixel intensities of on the order of 125 ADUs (based on a preliminary conversion from coarse and fine bits) or 7.5 photons at 17 Hz frame rate suggest charge deposits on the order of $3.4 \cdot 10^4$ e^-/s/pixel or roughly 140 photons/s/pixel. The noncollimated beam covers $\sim 30 \times 80 = 2400$ pixels, so this converts to $3.4 \cdot 10^5$ ph/s for the full beam's flux.

Conversely, the nominal filtered beam intensity is $\sim 1.5 \cdot 10^9$ ph/s. Behind the SiO_2 layers of the test chip, $\sim 1 \cdot 10^6$ ph/s remain, another factor $\sim$2 is lost in the chips' metallization layers. Thus, the PERCIVAL-measured beam intensity, based on preliminary calibrations, matches reasonably well the flux estimate from upstream P04 beam intensity measurements. Interim collimations of the beam by other, primary user, experiments (which are transparent to the central transmitted beam) prevent a more precise beam intensity measurement before entry into PERCIVAL's chamber.

6. Conclusions and outlook

The PERCIVAL soft X-ray imager promises high-performance imaging capabilities for a wide range of experiments at FEL and synchrotron sources. Its projected key performance parameters of up to 120 Hz frame rate, reliable single-photon counting simultaneous with a dynamic range extending to $\sim 10^5$ photons/pixel/frame, and large uninterrupted imaging area of 10×10 cm^2 with 27μm pixels adresses many needs of the communities wanting to make optimum use of today's light sources.

The front-illuminated test chips have passed functional tests, detailed characterization of their performance is underway. In parallel, these small test devices are being backthinned to enable evaluation of the soft X-ray performance. Soft X-ray testing of backthinned test devices will be performed in 2014, and a first full-size imager is planned for commissioning in 2015.

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