Irradiation and beam tests qualification for ATLAS IBL Pixel Modules

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Abstract

The upgrade for the ATLAS detector will have different steps towards HL-LHC. The first upgrade for the Pixel Detector will consist in the construction of a new pixel layer which will be installed during the first shutdown of the LHC machine (foreseen for 2013-14). The new detector, called Insertable B-Layer (IBL), will be inserted between the existing Pixel Detector and a new (smaller radius) beam-pipe at a radius of 33 mm. The IBL will require the development of several new technologies to cope with the increase of the radiation damage and the pixel occupancy and also to improve the physics performance, which will be achieved by reduction of the pixel size and of the material budget. Two different promising silicon sensor technologies (Planar n-in-n and 3D) are currently under investigation for the Pixel Detector. An overview of the sensor technologies’ qualification with particular emphasis on irradiation and beam tests are presented.

Keywords: ATLAS upgrade; Insertable B-Layer; IBL; FE-I4; Radiation hard sensors; NIEL; Planar pixel; 3D pixel

1. Introduction

The ATLAS detector is a general purpose detector [1] at the Large Hadron Collider at CERN, which was designed to be sensitive to a wide range of physics signatures to fully exploit the physics potential of the LHC collider at a nominal luminosity of 1x10^{34} cm^{-2}s^{-1}. After the successful commissioning and operation in the last two years, it is planned to extend the LHC physics program into the High-Luminosity LHC (HL-LHC) by increasing the instantaneous luminosity by a factor of five. A three-phase upgrade of the LHC will be followed along by the upgrade of the ATLAS detector. The first phase (Phase-0) will take place during the 20-months long shutdown in 2013-2014 and will include the LHC magnets’ repair to achieve the designed 14 TeV in the center-of-mass proton-proton colliding system. The instantaneous luminosity will reach 1x10^{14} cm^{-2}s^{-1} and an integrated luminosity of 50 fb^{-1}. The second phase (Phase-1) will take place during the second 12-months long shutdown in 2017-2018 and will aim at a further increase of the instantaneous luminosity up to 2x10^{14} cm^{-2}s^{-1} and an integrated luminosity ~ 300 fb^{-1}. The third phase (Phase-2) will take place after 2022 and will initiate the HL-LHC era aiming at 3000 fb^{-1} integrated luminosity to be collected during the following years.

During the Phase-0 shutdown the ATLAS Pixel Detector [2] will be extended with an additional layer inside of the existing detector system. The so-called Insertable B-Layer (IBL) [3] will be installed together with a new beam pipe to maintain an excellent vertex detector performance and compensate possible inefficiency of the current Pixel Detector, which may arise during the luminosity increase after the Phase-0 and Phase-1 machine upgrade.

This report is a follow up to [4, 5, 6, 7].

2. ATLAS IBL requirements

The ATLAS IBL will be the fourth pixel layer mounted on a new beam pipe inside of the current innermost Pixel Detector layer (B-Layer). It is designed [3] to have 14 staves equipped with 32 sensor-chip assemblies with the sensor side of the assemblies closer to the beam pipe. The distance to the collision axis of the IBL modules is to be 31 mm in the closest and 40 mm in the outermost points with a mean distance of 33 mm.

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The IBL Technical Design Report (TDR) [3] assumptions and module related characteristics are:

- The detector will operate until the Phase-2 upgrade, which implies a peak instantaneous luminosity of $2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ and an integrated luminosity of 550 fb$^{-1}$, or in terms of a total fluence $5 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$ including safety factors.
- A hit efficiency in the active area of the sensors greater 97% until after the total dose.
- Angular coverage: high $p_T$ tracks hit the sensors in IBL with a phi angle between 0° and 28° and an $\eta < 2.58$.
- A geometrical inefficiency < 2.6%.
- The target temperature for operating the IBL sensors is approximately -15° C, in order to minimize effects of reverse annealing on the sensors and to avoid thermal runaway. This also implies: an expected power dissipation < 200 mW/cm$^2$ at -15°, a sensor maximum bias at 1000 V, a leakage current < 100 nA/pixel.
- Technology driven engineering parameters: sensor thickness 225 ± 25 µm, small inactive edge < 450 µm (this implies a sensor having a slim or active edge).

For the IBL a new front-end chip, called FE-I4 [8], was designed in 130 nm CMOS technology and consists of 26880 pixel cells organised in a matrix of 80 columns (250 µm pitch) by 336 rows (50 µm pitch). The chip is using a 40 MHz clock and provides a digital readout with cell-wide adjustable threshold and internal 4-bit counter for the signal amplitude as Time over Threshold (ToT) measurement.

There are two different sensor design technologies which were chosen for the module construction. Depending on the technology, the modules consist either of one or of two sensor-chip assemblies. The planar pixel sensors (PPS) are manufactured by CiS (Erfurt, Germany) in n-in-n technology (200 µm thick) and are going to be mounted by two assemblies per module (Fig. 1a). The 3D sensors with double sided column structure (230 µm thick) are manufactured by FBK (Trento, Italy) and CNM (Barcelona, Spain) and have only one assembly per module (Fig. 1b). Shingling in $z$ is not foreseen for the IBL modules due to radial space constraints. This results in slightly different geometric acceptance for 2-chip and 1-chip assemblies. For 1-chip (2-chip) assemblies the nominal acceptance for particles normal to the beam was estimated to be 98.8% (97.4%) for 450 µm inactive edges. An air gap of 200 µm (100 µm) between two-chip (single-chip) modules has been assumed to take into account the higher bias voltages needed by PPS with respect to 3D sensor-chip assemblies.

The final IBL design for the Planar n-in-n technology by CiS employs:
- guard rings on p-side are shifted underneath the outermost pixels,
- inactive edge reached at 200 µm,
- less homogeneous electric field, but charge collection after irradiation dominated by region directly underneath the pixel implant.

The final IBL design for the 3D sensors produced by FBK and CNM is based on a similar process:
- FBK full pass-through columns stopped by membrane, using p-spray for pixel isolation, 200 µm inactive edge,
- CNM stop etching before reaching opposite end, columns 210 µm deep (out of 230 µm p-bulk thickness),
- same layout and column geometry in both designs,
- 10 µm column diameter.
Figure 1: The a) PPS and b) 3D - module design. a) The PPS modules are being assembled with two chips on a module with an additional spacing between the sensor-chip assemblies - 400 µm, to account for safe sensor operation at high bias voltage. b) The 3D modules contain only 1 sensor-chip assembly. The distance between the sensor edges being reduced to 100 µm. Figures from [3].

3. Irradiation and beam tests

In 2011 four testbeam campaigns were carried out. The first two took place at the DESY II synchrotron with a 4 GeV positron beam. In the beginning the beam time was dedicated to understanding the FE-I4 chip, which became available only shortly before the first testbeam at DESY. In the second DESY testbeam the first irradiated samples were tested. The beam tests of the sensor-chip assemblies in the magnetic field in the CERN Morpurgo [9] magnet at 1.2 Tesla were performed in June with 180 GeV pions. However the beam time was reduced (from 5 weeks to 5 days) due to machine problems. The IBL Review Committee took place in July for an inspection of the sensor development and readiness of the PPS and 3D sensor technologies for the IBL modules production. The IBL Review decision allowed both technologies to proceed. At the moment a dual-technology IBL is being evaluated so that both the PPS and 3D best features are used. The testbeam period in September at CERN in the beam of 120 GeV pions was dedicated to clarify questions raised by the Review Committee regarding the performance of the sensors.

The beam tests both at DESY and CERN were done using the EUDET telescope [10]. The FE-I4 assemblies were treated as Devices Under Test (DUT) and their readout was performed with a USBPix system [11]. The USBPix system data stream was sent via TCP/IP by one of the EUDET telescope DAQ software modules and stored on disk combining the particle hit information from the telescope sensor planes and the DUTs in one event. The DUT full DAQ integration approach described above simplified the subsequent track reconstruction. The final steps of data analysis were done in the TBMon program, which was a standalone software package based on ROOT [12]. TBMon was developed for fast histogramming of selected DUT-track interaction features, e.g. hit efficiency, track residuals, charge collection, and charge sharing.

3.1. Irradiation

The sensors were irradiated at fluences up to 5x10^{15} n_{eq}/cm^{2}:
- in the proton CERN PS beam at 24 GeV, or,
- in the proton beam at Karlsruhe at 23 MeV, or,
- with neutrons at TRIGA reactor in Ljubljana, which covers a relatively broad energy spectrum up to several MeV.
3.2. Leakage current, power dissipation and noise level

The leakage current and the power dissipation strongly depend on the sensor temperature. A set of measurements has been performed for 3D and PPS sensors to demonstrate their operational features after irradiation up to $5 \times 10^{15}$ n$_{eq}$/cm$^2$ and operated at the nominal IBL TDR temperature regime.

In a set of laboratory measurements it was shown that the operational voltage for 3D sensors increases from few tens of Volts (for non-irradiated sensors) to ~160 V (at $5 \times 10^{15}$ n$_{eq}$/cm$^2$). The optimal operation voltage provides high charge collection efficiency while maintaining low noise levels. The typical leakage current for a sensor irradiated to $5 \times 10^{15}$ n$_{eq}$/cm$^2$ at the operation voltage is about 200 µA (at -15°C), which corresponds to a power dissipation of about 10 mW/cm$^2$, well below the IBL TDR limit of 200 mW/cm$^2$. The leakage current and power dissipation grow linearly with fluence and show anticipated dependence on the temperature of the sensors.

The PPS IBL chip assembly temperature measurements were carried out with a PT-1000 temperature sensor glued directly to a 1-chip assembly. To represent a realistic annealing scenario during the IBL lifetime, the sensors were annealed for 2 hours at 60°C according to the qualification measurements plan. After annealing, the assemblies showed a leakage current of approximately 320 µA at 1kV of bias voltage and -15°C. Taking into account only the active area of the FE-I4, this translates into a power dissipation of about 93 mW/cm$^2$, much below the permitted 200 mW/cm$^2$. The leakage current recalculated per one pixel value amounts to about 12 nA/pixel, again well below the allowed 100 nA/pixel. Bias voltage scans of the irradiated planar sensors in the testbeam showed that for tracks normal to the sensor plane the hit efficiency can be kept high (>97%) at voltages as low as 600 V.

The sensor noise occupancy is defined as noise hit probability, i.e. the average rate of the pixels with the signal above the threshold which are being read out by the front-end chip, while there was no particle passing through the sensor. The noise occupancy measurement was performed [13] with no dedicated irradiation source by varying FE-I4 threshold value within the range which corresponds to collecting 1100 to 3200 electrons per pixel. Figure 2 presents the noise occupancy over the total pixel number for the PPS and the 3D sensors averaged over $3 \times 10^6$ random triggers. The tests showed that low threshold operations are possible at values below 1500 electrons, while this value was chosen as a conservative value for FE-I4 operation in the testbeam. The charge collected by the PPS and 3D sensor-chip assemblies irradiated to $5 \times 10^{15}$ n$_{eq}$/cm$^2$ was measured to be above 10 thousand electrons per pixel at normal incidence angle, which is significantly above the noise level (~50 times as high) and ~7 times as high as the threshold level.

3.3. Pixel efficiency

For both sensor technologies the required efficiency >97% at maximum NIEL ($5 \times 10^{15}$ n$_{eq}$/cm$^2$) and working temperature (-15°C) has been demonstrated for particles at incidence angle to the sensor normal $\Phi=0°$ (not tilted) and 15° (tilted). Figure 3 shows the hit efficiency map averaged over all active pixels. The plots include ~50% of the neighbouring pixels area from all sides for better visual apprehension of the pass-through electrodes effects. The hit efficiency drop due to the bias electrodes is clearly seen for not tilted 3D sensors (Fig. 3a), where the pass-through electrodes are parallel to the beam, and for PPS (Fig. 3b), where the inefficiency spreads over a relatively larger area at the bias electrode pixel edge. The hit efficiency recovery in the bias electrode area of the sensor is seen for the 3D sensors tilted at 15° to the beam and the overall pixel efficiency reaches ~99% (Fig. 3c). The PPS sensor efficiency
map for not tilted and 15° tilted (Fig. 3d) sensor show the overall pixel efficiency close to 98%. The PPS sensor efficiency map demonstrates the drop in the area of the bias electrode for both tilt configurations. Figures 3b,d show only the right-hand pixel relative to the bias electrode in the double column structure due to the symmetry in the efficiency.

The sensor edge pixel efficiency measurement can be considered as direct measurement of the size of inactive sensor edges (Fig. 4). The PPS edge pixels are twice as long as the ordinary pixels and stretch under the guard ring structure (Fig. 4a). There is no specific design for the 3D sensor edge pixels and they are identical to other pixels on the sensor (Fig. 4b). The measurement of the pixel efficiency in the direction of the sensor physical edge and the determination of the point where the hit efficiency drops to 50% allows the derivation of the size of the sensor inactive edge. The values obtained both for the PPS sensors, 215 µm (Fig. 4c), and for the 3D sensors, 200 µm (Fig. 4d), perfectly comply with the limit set by the IBL TDR, inactive edge <450 µm.

The preliminary analysis of the highly tilted sensor beam tests (corresponding to η=2.5) has shown similar or higher efficiencies for both sensor technologies. The results on the high η beam test analysis are being finalised and will be reported separately.

Figure 3: Pixel efficiency map for the sensors irradiated to 5x10^{15} n_{eq}/cm^2 and cooled to -15°C. The overall pixel efficiencies are almost equal for not tilted 3D (a) and PPS (b). The inefficiency area due to pass-through electrodes clearly visible for both sensor technologies and both tilt angles. For the PPS sensor the inefficiency zone is located at the bias electrode pixel edge and covers a relatively large area of the pixel. The 3D sensor tilt by 15° recovers the sensor efficiency by ~1.5%(c), while for the PPS (d) no effect is seen.

4. Summary

Following the LHC upgrade program towards the HL-LHC, the ATLAS Inner Detector will be upgraded in two steps. In this paper the first year sensor qualification program effort for the Insertable B-Layer (IBL) is described. The two pixel sensor technologies, the planar pixel and the 3D pixel, have been demonstrated to comply with the IBL TDR requirements and operate well after a high irradiation dose. The FE-I4 chip, developed to cope with higher occupancy at the ever increasing luminosity, showed very good performance during the beam tests. However, a deeper understanding of the chip is required for the final ToT calibration.

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Disclaimer

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Figure 4: The edge pixel layout of the a) PPS and b) 3D sensors (at different scales). Hit efficiency for edge pixel and the sensor inactive edge width shown for c) PPS (HV=1000 V) and d) 3D sensor (HV=160 V). The sensors irradiated to 5x10^15 n_eq/cm^2 were cooled to -15°C during the measurement.

References