Development of Edgeless TSV X-ray detectors

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ABSTRACT: We report about the activity and progress on the development of TSV edgeless detectors at DESY. One part of the development is Through Silicon Via (TSV) technology for the Medipix3RX readout chip (ROC). TSV technology is a concept of connecting readout chips to readout electronics. Instead of wire-bonding which introduces a large dead area, TSV enables connection through the ROC itself. By replacing wire-bonding with TSV, the dead space between detector modules will be reduced from around 7 mm to only 1.6 mm. The thickness of the wafer will be 200 μm, with a via diameter of 60 μm. Inside of the via, a 5 μm thick copper layer will be used as a conducting layer. On the back side of the chip a Redistribution Layer (RDL) will be deposited. For the RDL structure, 5 μm thick copper with 40 μm wide conductive lines will be used. Bump bonding of the sensor plus ROC assembly to ceramic readout board will be optimized in terms of material and bonding temperature. The second part of the project is the development of the edgeless sensor units using active edge sensor technology. Active edge sensors have been simulated with Synopsys TCAD for different polarities including p-on-n, p-on-p, n-on-p and n-on-n with p-spray or p-stop for different thicknesses from 150 μm to 500 μm. Results show that the bending of the electric field close to the active edge is leading to image distortion on the sensor edge. In addition, the current design of active-edge sensors shows very poor radiation hardness. We are currently working on the development of a radiation hard active-edge sensor with optimized imaging quality. The final goal of this development is to make Large Area Medipix Detector (LAMBDA) with TSV edgeless units.

KEYWORDS: X-ray detectors; Hybrid detectors; Through Silicon Via; Edgeless sensor.

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Contents

1. Introduction

Hybrid pixel detectors are the cutting-edge technology for many X-ray experiments at synchrotrons and Free Electron Lasers. The span of the applications extends from material analysis and biomolecular screening to chemical dynamics monitoring.

However, these detectors suffer from a certain amount of dead space between modules, due to the need for guard rings in the sensor and wire bond connections to the readout chip. A possible solution is to use detector modules with minimum inactive areas around the edges using active edge sensors and readout chips (ROC) with Through Silicon Via (TSV) technology.

The current state of the art includes the CERN TSV Medipix3 chip fabricated at CEA-LETI [1] and VTT (Advacam) edgeless X-ray sensor [2].

Our development starts with the LAMBDA detector (figure 1 and 2) which was designed and produced at DESY FS Detector Group in Hamburg, Germany [3]. The goal is to make TSV based slim edge LAMBDA detector units.

2. Through Silicon Via (TSV) technology basics

Deep Reactive Ion Etching (DRIE) is used for the formation of vias into silicon. To achieve a high aspect ratio and the etching of vertical sidewalls the so-called Bosch process was developed and is now state of the art for the TSV formation process. This etching process consists of two basic steps which alternate one after another. One step is the application of the silicon etching gas, mainly SF_6, which is applied for a short time by a plasma etching procedure. In this way a stud hole is made in the surface of the silicon. Next step is the application of the passivating polymer which will cover the surface of the stud hole and protect the walls of the growing via during further plasma etching. In the next step, plasma etching is applied again for a short period until the depth of the stud hole is increased and subsequently polymer passivation is employed to protect the walls from etching [4]. Alternating these two steps it is possible to drill a via in the silicon with vertical sidewalls and an aspect ratio of up to 20:1 which represents the depth of the via over the diameter of the via.

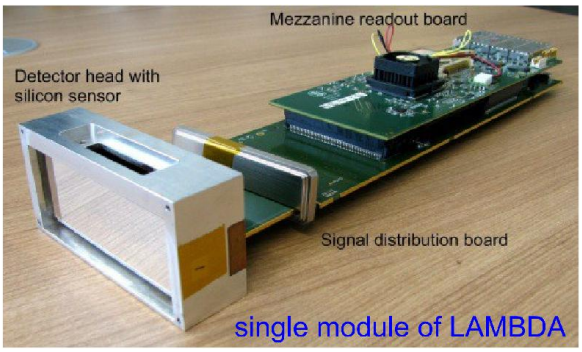

Figure 1. LAMBDA detector unit together with readout electronics.

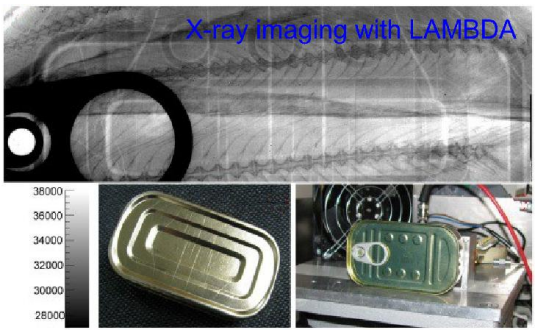

Figure 2. X-ray image taken with LAMBDA.

3. Medipix structure

The Medipix3RX readout chip is designed to be compatible with TSV technology. In one of the inner metal layers, M1, landing pads for TSV contacts are fabricated. TSV landing pads are square shaped, size 76.5 x 76.5 μm^2, with the pitch of 120 μm.

4. TSV formation process planned on Medipix3RX wafer

The technology steps involved in the production of Medipix3RX TSV modules are given in figure 3. The process starts with Under Bump Metallization (UBM) formation on the front side of a Medipix3 wafer, which includes the following steps: sputtering of the adhesion and seed layer, followed by photoresist lithography and deposition of UBM by electroplating of a Ni/Au metal layer stack. The next process is temporary bonding the front side of the Medipix wafer to a carrier wafer. Subsequently, the Medipix wafer is thinned to a thickness of 200 μm. Now, the TSV structure can be etched from the back side of the wafer by deep reactive ion etching (Bosch process) and the TSV sidewall and the wafer backside are passivated by an oxide layer. Openings in the passivation layers on top of the metal M1 are made in order to provide an electrical contact from the back side metallization and Redistribution Layer (RDL) to M1. The conformal via filling and RDL formation are realized by electrodeposition of a 5 μm Cu layer. On top of the copper layer a polymeric interdielectric layer is deposited and patterned followed by the electroplating of the final Ni/Au pads for the chip to board interconnection. Finally, the carrier wafer is de-bonded and Medipix wafer front side is cleaned. At this point the Medipix wafer is bonded to the support wafer on the back side which will give mechanical stability during flip chip assembly. Afterwards, the wafer stack is diced and chips are sorted according to their optical and electrical classification. The structure of the finished readout chip in respect to the TSV is given in figure 4.

5. Redistribution Layer (RDL)

The RDL is designed to serve as an interconnection between TSV contacts and Bump Bonds which should connect to the detector readout board. The material of the RDL is copper, 5 μm thick with line width of 40 μm per TSV. The smallest distance between conductive lines is

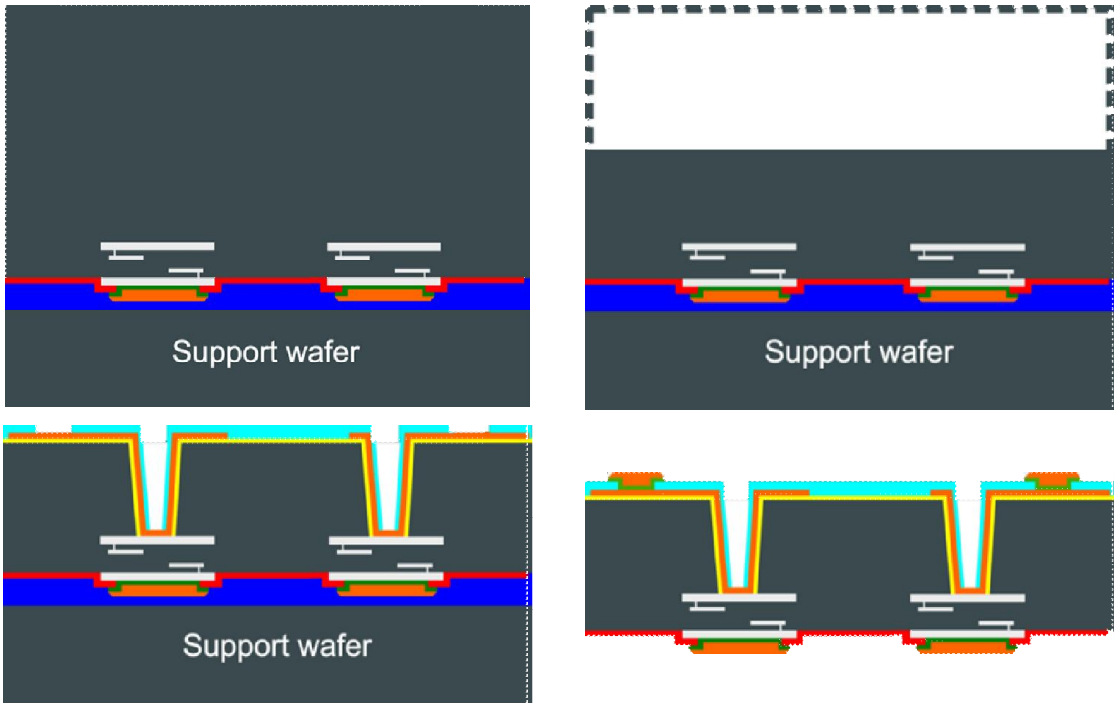

Figure 3. Technology steps involved in the production of the Medipix3RX TSV module. Top left: Medipix3RX wafer, thickness 725 μm, after UBM deposition on the front side and bonding to carrier wafer. Top right: Medipix wafer after thinning. Bottom left: Wafer after TSV etch from the back side, passivation, TSV Cu filling and back side RDL. Bottom right: Wafer after UBM metallization on the back side and de-bonding of carrier wafer and cleaning of the front side.

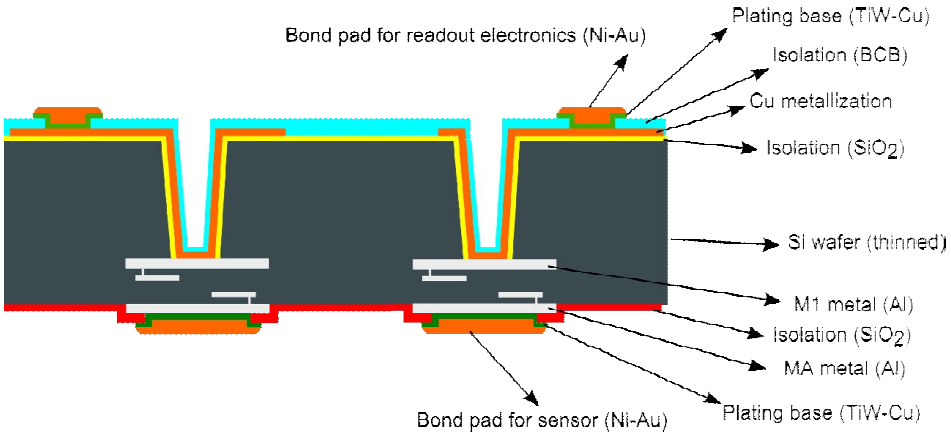

Figure 4. Final structure of the Medpix3RX TSV readout chip (not to scale).

40 μm while spacing between differential pair lines is 25 μm. The RDL is designed with special emphasis on signal integrity of differential pairs. The number of TSVs is 114 while the number of bump bonds is 70 which form the matrix of 7x10. Therefore, some of the TSVs are connected to the same bump bond in the Ball Grid Array (BGA) in order to reduce the number of bumps and leave more space for wiring. Figure 5 gives the routing map of the RDL (left) and calculated distribution of the resistance of the lines from each via to the specific bump. Calculacion is done taking into account width of the lines, length and thicknes, together with copper resistivity. Resistance is in the range from zero to two ohms. Table 1 gives calculated power dissipation and voltage drop per specific power and corresponding ground. Dissipation is

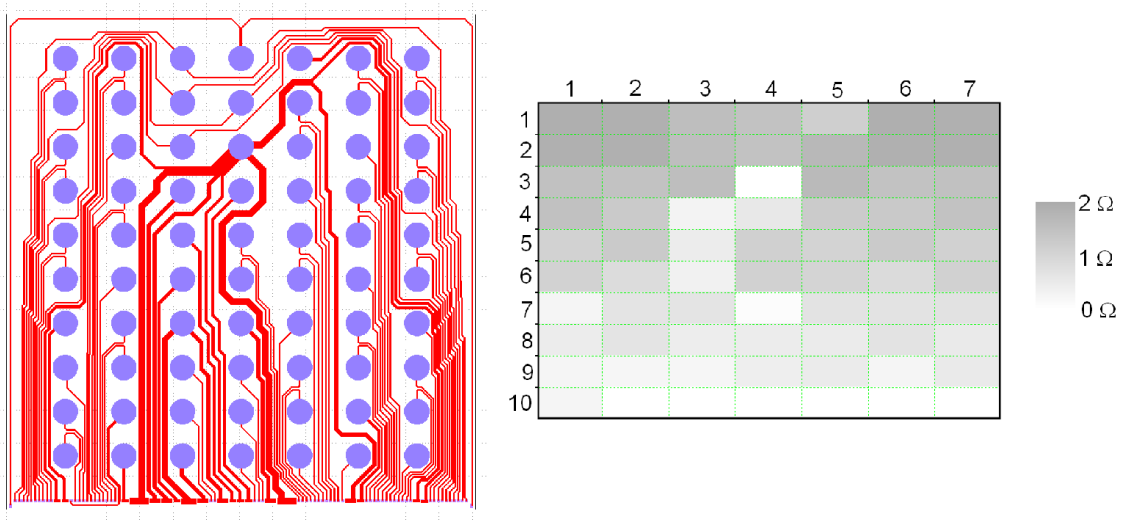

Figure 5. Structure of Redistribution Layer (left). Resistance of the conductive lines from particular via to the specific bump bond (right). Zero ohm is indicated with white color and 2 ohms with black.

Table1. Resistance, power dissipation and voltage drop depending on the specific power or ground calculated for RDL layer given in figure 5.

Power/Ground	Bias [V]	Resistivity [Ω]	Max. current [mA]	Power dissipation [mW]	Voltage drop [V]
VDDA	1.5	0.0325	664	14	0.0215 (1.4%)
GNDA	0	0.0523	664	23	0.0347 (2.3%)
VDD	1.5	0.022	170	0.6	0.0037 (0.25%)
GND	0	0.0298	170	0.8	0.005 (0.34%)
DVDD	2.5	0.05	51.4	0.13	0.0257 (0.1%)
DGND	0	0.103	51.4	0.27	0.0053 (0.2%)

on the order of 10 mW which is acceptable since power consumption of Medipix3RX chip is around 1W and most of this energy is transformed into heat so RDL would add to the total dissipation only around 1%. Voltage drop is on the order of 1% of input bias which is again acceptable in the sense of signal integrity. Calculations are made for the worst case scenario of maximum current which is given in table 1 and taken from Medipix3RX manual.

6. Development of edgeless silicon sensors

Recent advances in active-edge technology enable the development of edgeless silicon sensors. The main processes involve Deep Reactive Ion Etching for creation of a deep trench surrounding all active pixels and edge implantation for prevention of the leakage current generation by defects at the edge. At DESY, we are aiming for the development of radiation-hard edgeless silicon sensors based on active-edge technology for photon science applications. To have a cost-saving development, our strategies are: firstly, investigating the radiation hardness of edgeless sensors from available commercial designs according to the TCAD simulation with X-ray radiation damage parameters implemented; secondly, based on the understanding of results from available designs and previous experience obtained from the

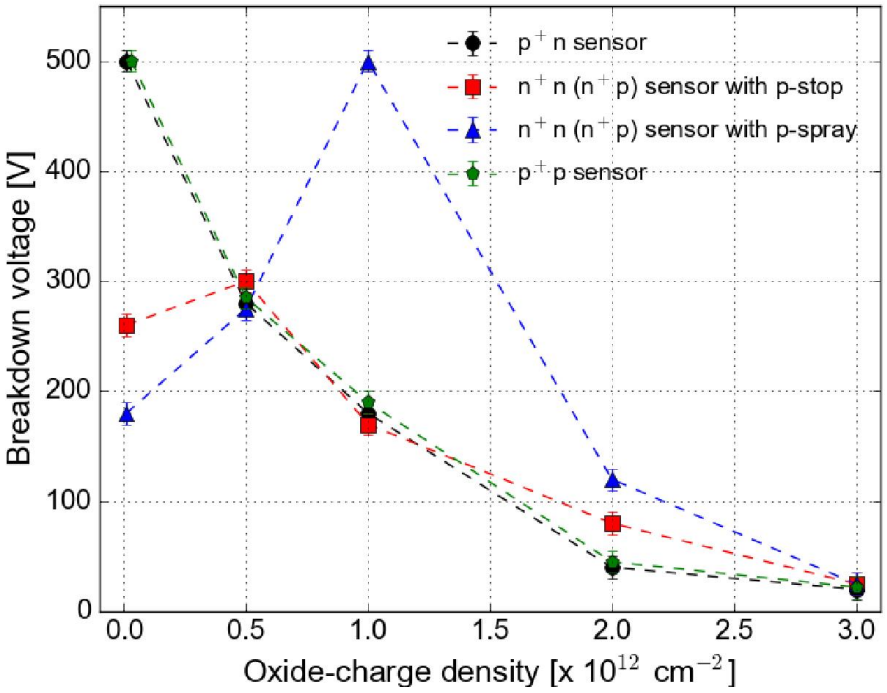

Figure 6. Breakdown bias vs. oxide charge density for different types of the sensors.

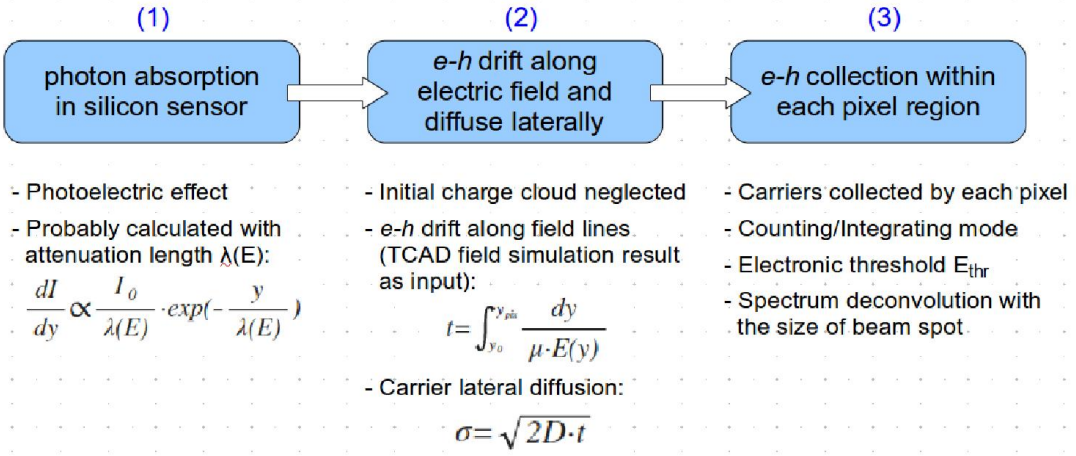

Figure 7. Process flow for the calculation of the charge collection at the edgeless sensor.

development for AGIPD sensor [5], optimizing the sensor layout for radiation hardness; finally, optimizing the edge structures to achieve better charge collection for pixels close to the active edge.

The radiation hardness of edgeless sensors has been investigated through TCAD simulations. The edgeless sensor has a pixel pitch of 55 μm and a distance of 50 μm from the last pixel to the active edge. The thickness of the field oxide layer is 700 nm and the pixel junction depth is 1.2 μm, which are critical for sensor breakdown after a high-dose irradiation. In this simulation we consider various models: drift-diffusion model, mobility model with degradation at interfaces, Shockley-Read-Hall (SRH) recombination model with carrier lifetime

of ~1 ms, and avalanche model. In addition, oxide-charge density and surface-recombination velocity, which represent the parameters related to X-ray radiation damage, were implemented in the simulation for the breakdown voltage of the edgeless sensor. The simulations have been done for different sensor polarities, for example p-on-n, p-on-p, n-on-n and n-on-p with either p-spray or p-stop, and for different sensor thicknesses. From the same set of simulations, it was discovered that the breakdown voltage is not sensitive to different sensor thicknesses, thus only results for 300 μm thick sensors will be shown.

Figure 6 shows the simulation results on the breakdown voltage as function of oxide-charge density for different sensor polarities. For a high oxide-charge density of $3x10^{12}$ cm^{-2}, which is equivalent to ~10 MGy dose, all sensors show a very small breakdown voltage of about 20 - 25 V. Results indicate that none of the current designs can survive high radiation dose. However, it should be noted that, for n-on-n and n-on-p sensor with p-spray, the breakdown voltage increases with irradiation in the beginning and reaches a maximum at the oxide-charge density of $1 \times 10^{12} cm^{-2}$, figure 6. For the sensor with p-spray layer, the integrated dose of the dopants inside of this layer is about $1x10^{12}$ cm^{-2}. With increasing oxide charges to this value, the effective carrier concentration below SiO_2 decreases due to the compensation effect between excessive holes produced by p-spray dopants and electrons induced by oxide charges, which results in an increase of breakdown. The maximal breakdown is expected to appear at the oxide charges approximately equivalent to the p-spray dose. We do not expect a sharp pronounced peak in the sensor with p-stop with respect to the sensor with p-spray as no compensation effect is foreseen below SiO_2. By optimizing the p-spray dose for n-on-n and n-on-p sensor, it is possible to achieve a higher breakdown for high radiation dose. The optimization for p-spray dose for the improvement of sensor radiation hardness is still in progress.

Charge-collection studies of edgeless sensors given by R. Bates et al. [6] have shown a non-uniform charge collection by pixels close to the active edge. The behaviour can be explained by the strong bending of electric field close to the edge due to the presence of edge implant, which changes the electric field distribution in this region. To understand this in details, we have developed a model, which considers the photo absorption in silicon, creation of electron-hole pairs, drift of free carriers along the electric field and their lateral diffusion, charge collection by each pixel, and the functionalities of ASIC chips including photon-counting or charge integration and threshold settings. Figure 7 shows the process flow in the model calculation. The model calculation has been proven valid through a comparison to measurement results given by R. Bates et al. [6]. Details of the developed model are given by J. Zhang et al. [7]. It can be concluded that the charge-collection behaviour of edge pixels depends on the sensor thickness and the X-ray energy. For the current distance from the last pixel to the active edge, the last few pixels close to the edge cannot see low-energy photons (< 10 keV). In order to guarantee the sensitivity of last pixels to low-energy photons, we propose the distance from the last pixel to the active edge should be kept at least 50% of the sensor thickness.

7. Conclusion

A Through Silicon Via formation process for Medipix3RX readout chip wafers and the dimensions of the TSVs are developed. The TSV design is made according to the state of the art technology available at IZM Fraunhofer Institute in Berlin, Germany. The aspect ratio of the TSV is designed to be around 3:1 with 60 μm via diameter and 200 μm depth.

The RDL layer is designed as a single layer with a wiring structure which keeps the signal integrity of differential pairs. The power dissipation and voltage drop in this design are kept low.

Edgeless sensors with active edge technology and commercial design have been simulated and it has been shown that they do not satisfy requirements of radiation hardness and edge pixel charge collection.

Further development will be in the direction of TSV signal integrity investigations, detector substrate design for LAMBDA TSV units and a new design of the radiation hard sensors.

Acknowledgments

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