Vertically Integrated Circuits: Example of an Application to an x-ray Detector

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***Abstract*—Replacing planar circuits with vertically integrated ones allows to increment circuit functionalities on a given silicon area, while avoiding some of the problems associated with aggressively scaled technology nodes. This is particularly true for applications likely to subject circuits to high doses of ionizing radiation (such of x-ray detectors to be used in synchrotron rings and Free Electron Lasers), since the degradation mechanisms of some of the innovative materials to be used in most recent nodes have not been fully characterized yet. In this paper, an evolution is presented for the readout ASIC of a pixelated x-ray detector to be used for such applications. The readout circuit is distributed in a stack of two vertically interconnected tiers, thus doubling the circuitry resident in each pixel without increasing the pixel pitch (and thus compromising spatial resolution of the detector). A first prototype has been designed and manufactured, using a commercial 130nm CMOS technology. Design issues are discussed, along with preliminary characterization results.**

Keywords—3DIC; Vertically integrated circuit; AGIPD; x-ray detector; FEL

I. INTRODUCTION

The increase in functionality density of electronic circuits has up to now been achieved mainly by dimension scaling of devices and interconnections. Even if the number of available metal levels has increased with the evolution of technology, circuits have remained substantially planar. With the evolution toward more aggressively scaled technology nodes, novel materials have to be adopted (high-k gate dielectric, low-k inter-metal dielectric, metal gate, etc.), and further material substitutions will have to be needed the near future [1]. This is a potential problem for those application in which the circuits are exposed to conditions likely to impact device performances (like high level of ionizing radiation), since the most common degradation mechanisms (as defect generation or charge trapping) have been extensively characterized for traditional materials (Si, SiO_2), but not yet for the novel materials.

An example of such applications can be found in readout circuits for x-ray detectors to be used in Free Electron Lasers (FEL). The European X-ray Free Electon Laser (EuXFEL, [2]) facility, for example, is scheduled to produce x-ray pulses with a peak brilliance of about 10^{33} photons/(s mm^2 mrad^2 0.1%BandWidth), about 9 orders of magnitude more that 3rd generation synchrotrons. Readout circuits employed there will be exposed to a high level of ionizing radiation. Even if most of it will be absorbed by the sensor used for photoconversion, it is estimated that the readout ASICs will be subjected to a total ionizing dose of 10 to 100 MGy in a 3-year lifetime.

The EuXFEL will generate trains of 2700 x-ray pulses separated by 220ns: the pixelated detectors to be used in such a facility will have to acquire bursts of images at 4.5Mframe per second. To achieve that, most of the detectors developed for the task [3,4,5] adopt the approach of storing images on-pixel, delaying their actual sequential readout to a later time. Since spatial resolution desiderata impose a limit to pixel dimensions, dense integration of signal-processing and memory-storage circuits is a critical issue.

II. THE (2D) ADAPTIVE GAIN INTEGRATING PIXEL DETECTOR

The Adaptive Gain Integrating Pixel Detector (AGIPD) project is a collaboration between DESY, PSI, Universities of Bonn and Hamburg to develop a hybrid pixel detector (compatible with single photon sensitivity at 12 keV) to be used at the European X-ray Free-Electron Laser Facility. The sensor will consist of a 1Mpixel hybrid pixel detector; the readout will be performed by means of 16x16 ASICs, each composed of 64x64 pixels with a 200μm pitch.

To get both large dynamic range (up to 10^4 12keV photons per pixels per frame) while retaining resolution better than the one imposed by Poissonian statistics, a dynamically adjustable charge sensitive amplifier is integrated inside each pixel, able to reduce the preamplifier gain over 2 orders of magnitude if an excess of charge is collected: this is achieved by dynamically adjusting the feedback capacitor in a charge-sensitive preamplifier circuit [6]. The signal is passed to a Correlated Double Sampling (CDS) stage and then temporarily stored in the in-pixel memory, along with information pertinent to the preamplifier gain used. The image acquisition task is completed in less than 220ns, allowing the detector to be ready

for the next pulse in the train. When the pulse train has expired, stored images are read out sequentially through an output buffer. A schematic of the AGIPD pixel is shown in Figure 1.

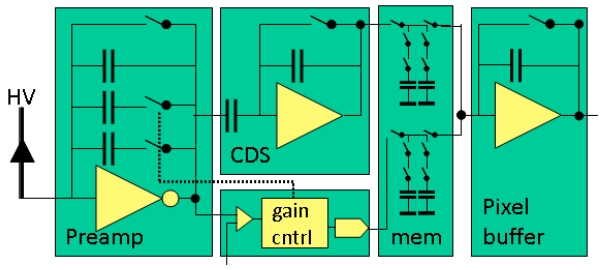

Fig. 1. Schematic of the AGIPD pixel.

Several prototypes have been produced on a reduced scale (16x16 pixels), along with a full-scale readout ASIC (64x64 pixels), using a commercial 130nm CMOS technology. All have been bump-bonded to silicon sensors, and have been tested both with laboratory x-ray tubes and at synchrotron facilities [7]. Results confirm the adaptive gain preamplifier concept to work correctly over a 10^4 12keV photons dynamic range and estimate a system noise compatible with single photon discrimination (<300e rms). The latest prototypes have also been irradiated to a dose exceeding 10MGy, confirming good operation after heavy irradiation.

Over 95% of the (200x200μm^2) pixel area is devoted to memory storage, but radiation tolerant design techniques (use of Enclosed Layout Transistors, guard rings around critical components) had to be employed in order to counter radiation-induced effects that would compromise detector performance. As a result, the system is able to store in its in-pixel memory bank up to 352 images, out of the 2700 possible images that could be provided by a full EuXFEL pulse train.

A veto scheme is developed as a partial solution, to overwrite memory cells storing non-interesting data, and thus increasing the effective memory depth. It would be desirable, however, to increase the memory depth further, without compromising spatial resolution and radiation tolerance.

III. A Vertically Integrated Evolution for the AGIPD Detector

In order to increase the memory depth, one possible solution would be to move toward more advanced technology nodes. If the node is not too-much aggressively scaled, this could even marginally improve the device radiation tolerance, as the oxide thickness reduction facilitates the annealing of trapped charge. The solution has however some drawbacks: the supply voltage reduction, for example, makes more difficult to achieve the same resolution (since the circuit has to map the dynamic range to a narrower voltage swing) and the use of innovative materials adds a significant degree of uncertainty to the post-irradiation behaviour of the system.

An alternative solution is to evolve the readout ASIC to a stack of vertically integrated layers, exploiting the additional silicon area to increase the memory storage capability.

A. Prototype and Technology Description

The long-term goal of the development presented here is to arrive at the definition of a multi-tier stack, in which different layers are optimized for different tasks, and the memory depth is increased up to 2700 images. Present limitations on technology availability, however force us for the moment to use a stack of just 2 tiers, manufactured using the same CMOS process, thus also limiting memory depth to a lower number.

A prototype has been designed and produced on a Multi-Project Wafer (MPW) via CMP [8], using a commercial 2D CMOS technology (Global Foundries 130nm CMOS Low Power) and post-processed by Tezzaron [9] to produce a 3D Integrated Circuit (3DIC). The prototype is shown in Figure 2.

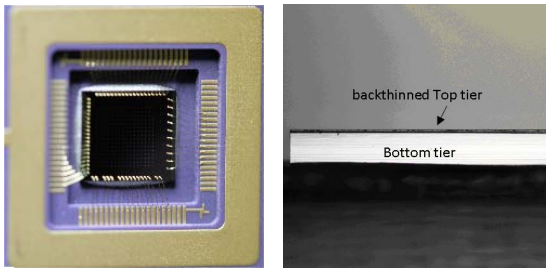

Fig. 2. Picture of the 3D-AGIPD0 prototype from the top (left picture) and from the side (right picture).

The vertical integration process consists in the manufacturing of 2 planar devices, with the definition of Through-Silicon Vias (TSV) as a "via-middle" step. The two tiers are then stacked and coupled face-to-face, and the Top tier is back-thinned to expose the TSVs, over which pads are formed to access the circuitry from the outside.

The tiers are kept together by an array of octagon-shaped metal structures (bondpoints) in the top metal layer: when the layers are stacked together, corresponding metal bondpoints on the opposite tiers are joined, giving the system both mechanical stability and the possibility of tier-to-tier communication (since circuitry residing in a tier can be put in contact to a bondpoint by means of regular metal vias, and that bondpoint is in electrical contact with its correspondent bondpoint in the opposite tier). An example is shown in Figure 3.

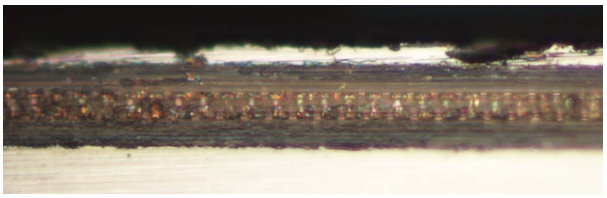

Fig. 3. Section of 3D-AGIPD0 prototype, showing tier-to-tier bondpoints.

The result is a pixel array in which each of the pixels is actually a "sandwich" of two functional units, one fully dedicated to memory storage, while the second being a mixture of signal processing circuits and memory storage.

B. Prototype Design and Layout

The signal, arriving from a bump-bonded external sensor, is to be passed through a TSV to a preamplifier (simplified

respect to the standard AGIPD one), and then a CDS stage. A tier-to-tier set of contacts (redundant to lower the resistance on the analogue signal path, and to prevent eventual misalignment-related issues) allows each pixel in one tier to communicate with the other tier, so that the processed signal can be routed to one of two analog memory batteries (distributed between the two tiers, for a total memory depth of 544 images). The signal can later be recovered by an output amplifier, and then be sequentially read out (Figure 4,5). Additional tier-to-tier contacts are included, to address the proper storage cell during the acquisition and read-out phases.

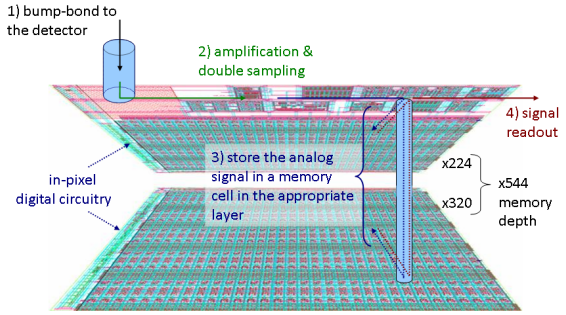

Fig. 4. Sketch of the 3D-AGIPD0 prototype pixel, distributed between two vertically integrated layers, for a total memory depth of 544 images.

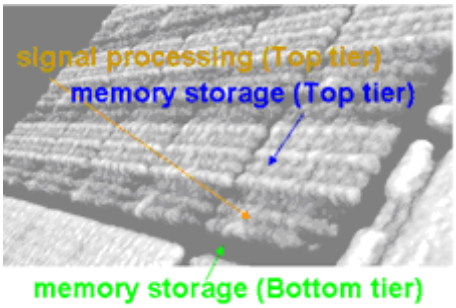

Fig. 5. X-ray tomography of 3D-AGIPD0 prototype. In the periodic pxel structure, the three basic pixel components (Top memory, Bottom Memory, signal processing circuitry) can be recoglized because of their different interconnect metal densities.

The purpose of this first prototype was to verify the feasibility of this kind of 3D integration, rather than to provide a maximum-performance sensor: thus, no serious effort has been put in minimizing the area used for in-pixel signal processing circuitry. On the opposite, additional digital circuits have been embedded in-pixel, to maximize testability of tier-to-tier communication. This resulted in a less-than-optimal pixel area occupation, which explains why the memory depth has not been increased to more than 544 images.

Most of the silicon area in the 3D-AGIPD0 prototype consists in a 16x16 array of the vertically-integrated pixels described above. The pixel array has a dedicated addressing logic, synthesized using the technology-provided Standard Cell Library. This digital circuit is distributed on both tiers, both at the pixel level and at the array level. In absence of a commonly accepted standard design flow for 3D digital circuits (and commercially available tools for 3D digital design), workarounds had to be devised, to define the circuit and place&route it using standard digital design tools developed for planar (2D) circuits (SDI Encounter). The approach used was to partition the circuit behavioural description in two verilog files (one for each tier), and synthesize them independently. To assure tier-to-tier contact, an ad-hoc standard cell was designed, compatible with the bondpoint array layout periodicity, and such "tier-to-tier contact" cells were pre-placed before the place&route phase of regular standard cells.

In addition to the pixel array and its addressing logic, test circuits (both 2D and 3D structures) have been embedded in the prototype, as well as daisy chains of TSVs and tier-to-tier contacts to evaluate the process yield. A floorplan of the prototype (in its two constituent tiers) can be seen in Figure 6.

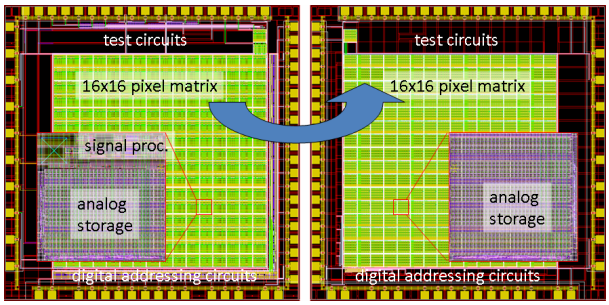

Fig. 6. Floorplan of the 3D-AGIPD0 prototype.

IV. Preliminary Test Results

Ten packaged samples (along with a higher number of unpackaged ones) have been received from the MPW consortium, and they are under test at the moment. Preliminary tests show reasonable yield figures, and confirm the feasibility of the approach proposed.

A. Through Silicon Vias

The TSVs are a critical component of the technology to be evaluated, since every signal to or from the external world has to pass through a TSV. In order to evaluate TSV yield, a daisy chain structure of 64 TSV connected in series was included in the prototype, and measured independently on each of the 10 packaged samples. None of the chains was found to be broken, and all showed similar resistance values, on average 2.1 ohm per TSV (as shown in Figure 7).

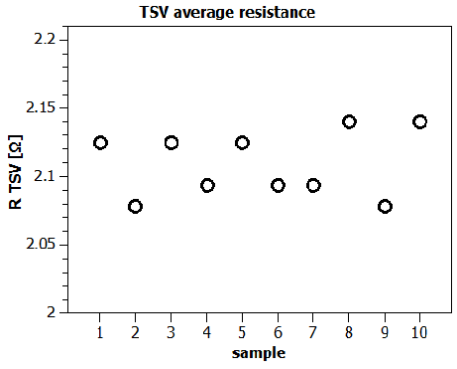

Fig. 7. TSV daisy chain test: all structures were found unbroken, having similar average resistance values.

B. *Tier-to-tier contacts*

As stated above, the tiers communicate by means of metal bondpoints facing each other. An eventual misalignment between the two tiers would be problematic, since it would break connection between bondpoints supposed to face each other, and eventually create connections between bondpoints which are not supposed to: in other words, it would cause open circuits and possibly shorts in the 3D circuit. Such problem (which had plagued the process in a former MPW run using this technology) can be corrected by introducing redundancy (and respect distances) in the tier-to-tier contacts, and this approach has been adopted in the 16x16 pixel array.

In order to evaluate the alignment accuracy (and the bondpoint contact reliability) in the present MPW, however, a daisy chain structure of 1000 tier-to-tier contacts connected in series (no redundancy) was included in the prototype, and measured independently on each of the 10 packaged samples. None of the chains was found to be broken, and all showed similar resistance values, on average 0.3 ohm per tier-to-tier contact (as shown in Figure 8).

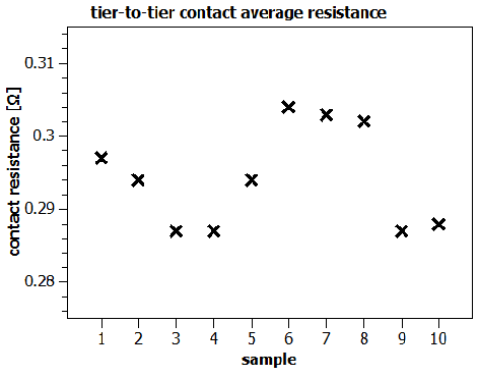

Fig. 8. Tier-to-tier contact daisy chain test: all the structures were found unbroken, having similar average resistance values.

C. *Active Circuits*

2D and 3D active circuits were measured independently on the 10 packaged samples. In 7 out of the 10 tested samples, the active circuit test structures were found to behave as expected.

Regarding the misbehaving samples, in one case it was found that the sample was presenting a very low current draw from the supply voltage pad, suggesting supply voltage was actually not provided to some circuits (likely because of a broken metal line), thus explaining their lack of response. In a second misbehaving sample, a transition was observed in the circuit behaviour, which was originally working as expected, and stopped to do so after a test period. This hints to a reliability rather than to a yield issue, and we suspect ESD to have been accidentally caused while handling the sample.

D. *16x16 pixel array*

In order to verify the functionality of the vertically integrated structures, tests were performed on the 16x6 pixel array, mimicking the write/read detector cycle. The CDS buffer has been used to charge randomly chosen memory circuits, both on the Top and the Bottom Tier. This has been repeated several times, storing the images in the memory banks; then they have been sequentially read out. In the operating range of the circuit, the output has been found to follow linearly the input (as it was expected), and it has been confirmed that images can be successfully stored in (and retrieved from) either of the memory banks (Figure 9).

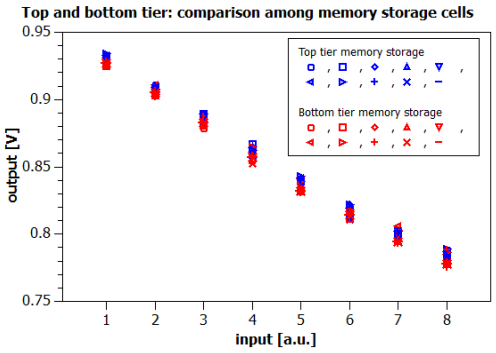

Fig. 9. Pixel array: comparison of the output when storing images in the Top tier memory bank or in the Bottom tier memory bank.

V. CONCLUSIONS

A 3D evolution for the readout ASIC of the AGIPD detector is being developed. A first prototype has been designed and manufactured in a 130nm commercial CMOS technology, distributing the readout circuit in a stack of two vertically interconnected tiers.

In absence of an accepted standard design flow for 3D circuits, workarounds were devised, to define the circuit using standard digital design tools developed for planar (2D) circuits.

Preliminary tests show good characteristics of TSVs and tier-to-tier contacts, as well as a reasonable yield of the active circuits. Key components located in the different tiers were found to behave in a similar way, and functionality of the vertically integrated structures has been confirmed.

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