

FIRST TESTS WITH THE SELF-TRIGGERED MODE OF THE NEW MICROTCA-BASED LOW-CHARGE ELECTRONICS FOR BUTTON AND STRIPLINE BPMS AT FLASH

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Abstract

The FLASH facility at DESY is currently enhanced by a second beamline (FLASH2) to extend the capacity for user experiments. In addition, certain support systems like the timing system and the BPM system at the existing FLASH accelerator have been partly renewed and are now under commissioning. New button BPM electronics based on the MTCA.4 for physics standard is provided for the FLASH2 beamline and is foreseen as a replacement of the old BPM electronics at FLASH. Compared to the predecessor of the FLASH button BPM electronics, the new system has been specifically designed for low charge operation exceeding a wide dynamical charge range between 100pC and 3nC. Special provisions have been made to enable single bunch measurements in a self-triggered mode, enabling timing-system-independent measurements during commissioning and at fallback during normal operation.

INTRODUCTION

The new 4th generation FEL light source FLASH2 puts high demands on the stability of the electron beam. Currently existing button and stripline beam position monitors (BPM) at FLASH deliver beam position measurements at a dynamic range for bunch charges down to approx. 0.3-0.5 nC, while machine operation at lower charges showed insufficient BPM resolution [1]. New MicroTCA-based low-charge BPM (LCBPM) electronics, currently under development and commissioning at FLASH2 enable measurements at a wide dynamic bunch charge range even down to <100pC. They are also intended as a replacement for the current FLASH BPM electronics. First tests at FLASH showing the properties of an adequate prototype RF-frontend have been presented at [1].

TEST SETUPS

The new LCBPM electronics are based on the delayline-multiplex-single-path-technology (DMSPT), developed for the HERAe-BPMs [2]. The new development incorporates substantial conceptual upgrades for increased performance and operational flexibility [1]. An Arbitrary-Function-Generator (AFG) was used for generation of single bunch-triggers or complete pulse trains. The AFG can alternatively be triggered externally from an accelerator timing-system board (X2Timer) located inside the LCBPM MicroTCA crate for tests of timing-coupled acquisition modes. The bunch-trigger generated by the AFG triggers a programmable button-

pulse generator that delivers two pairs of button-type buffered output signals per bunch into a DMSPT-delayline-combiner structure as described in [1]. Two of the output button-signals are chained by use of a DMSPT-structure each, to produce both button-pulse signal-chains for each of the two transversal BPM planes (x, y), connected to the x- and y-inputs of the MicroTCA Rear-Transition-Module (RTM). One of the four button-type signal paths contains a switchable step attenuator for the simulation of position offsets.

LCBPM AND TIMING SYSTEM

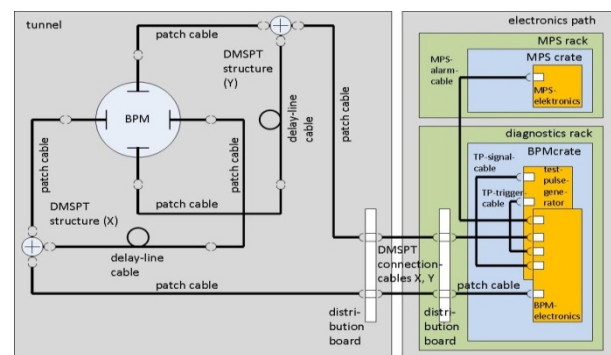


Figure 1: block diagram of the LCBPM channel setup.

An overview block diagram of a typical LCBPM channel setup is shown in Figure 1.

Delivery of arbitrary bunch pattern is supported by the new FLASH/XFEL timing-system [3], currently under commissioning at FLASH. The accelerator timing-system uses a special AMC card (X2Timer) for distribution of triggers, clocks, events and timing data to each individual timing-system-dependent card in the same crate. The LCBPM receives timing information from this board by means of dedicated MicroTCA crate backplane signals and uses this information according to parameterise to its own operation mode [4].

AUTONOMOUS OPERATION

LCBPM systems can operate in timing-system independent modes, the so-called autarchic modes (AT) as well as driven by the timing-system (TS).

At autarchic modes, a continuous data stream of 16-bit integer values is delivered at the digitizer sampling rate (125 MHz) from the ADC channels towards the FPGA, providing the RTM output signals received from the preceding pulse detection and signal conditioning stages.

Depending on the configuration of the timing-system, trains of bunches are repetitively generated based

according to the timing events. Since the LCBPM system is a true single bunch BPM, it is capable of triggering, measuring and storing the position of every bunch of the bunch train in separate memory locations. The measurement data is transferred from the LCBPM digitizer (SIS8300 [5]) via dedicated PCIe links to the CPU for read out by the device server. Each LCBPM channel is configurable by parameters via the PCIe bus.

In the autarchic modes the LCBPM continuously observes the incoming raw data stream from the SIS8300 digitizer card. If configurable level-related and temporal trigger conditions are met, a discharge pulse is initiated synchronously to the incoming initial button pulses for synchronous discharging of the peak detectors for the next and subsequent incoming bunches. In parallel to the initialization of the internally detected bunch-repetition-rate used for synchronous discharge and bunch-related measurements, raw data are synchronously stored and processed, related to subsequently measured bunches. Each block of data corresponding to the button pulses of a triggered bunch is put into the digital signal processing chain for further data processing. Transverse bunch positions are calculated based on the well-known Δ/Σ equation [2] [1]. Threshold- in combination with time frame-detection is used in the transverse X-Y-plane, to implement a triggering scheme, able to distinguish between spurious noise events and real signals from the BPM.

Measurement data and readout

Due to the limitations of the current MicroTCA infrastructure & interface firmware library (1_2_1), the LCBPM output data was organized in four separate buffers:

- the bunch data buffer (B), holding the bunch correlated measurement data (relative bunch-slot-nr, relative bunch-nr, bunch acquisition status, X-position, Y-position, sum-value),
- the macropulse buffer (M), holding all autonomously acquired macropulse-related status information (e. g. the relative macropulse nr),
- transverse plane raw data buffers (X, Y), containing transverse raw input-data according to the currently selected recording mode: in RS recording-mode, these buffers contain raw-data of a selected time-interval, while in RB recording mode raw-data of all acquired bunches will be delivered in these buffers. Disabling of the X- and Y-buffers is possible in R0 recording-mode to reduce the amount of data transfer via the PCIe bus.

MEASUREMENTS AND SYSTEM PERFORMANCE

The following Figures 2 to 5 show measurement examples as delivered by the LCBPM device server on a train of 6 bunches, x-position offsets of approximately 3 mm at typical frontend signal levels.



Figure 2: bunch train raw signals of 6 DMSPT-formatted bunch pulses at the LCBPM digitizer input (upper signal = x; lower signal = y direction).

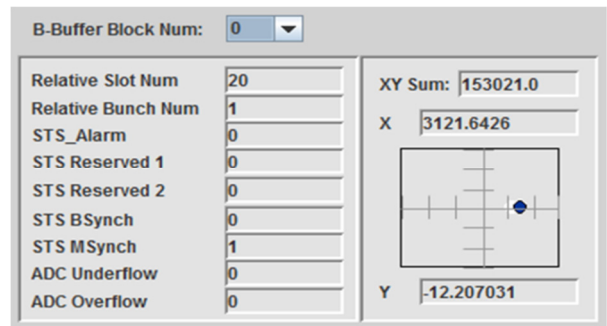


Figure 3: LCBPM position measurement and status information of the first bunch in the bunch train (x [μm], y [μm], XY Sum [a. u.]).

All further bunch data acquisition and measurement sequence is similar for the autarchic (AT) and the currently implemented primary timing-coupled (TS) mode as shown in Figures 2 to 5.

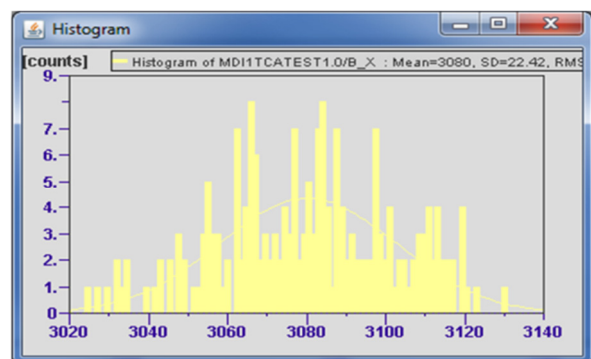


Figure 4: histogram of all x-position measurements of the first bunch showing quasi-random sample distribution (includes contribution due to sample distribution of signal source).

As the test setup mainly delivers a x-position offset, the histogram of Figure 4 shows a typical unsuspecting x-position distribution. As can be estimated from Figure 4, the typical measurement resolution in a test-system will be in the range of 20-30 μm , including the contributions due to the sample distribution of the signal source itself. It

has sub-micrometer granularity and it was found in test setup measurements that the x- and y-resolutions seem to be independent of the absolute position readings, as long as the bunch position is smaller than the corresponding monitor constant. This position measurement resolution meets the performance specs (50 μm) as formerly defined by the needs of the FLASH2 accelerator coordination team [6].

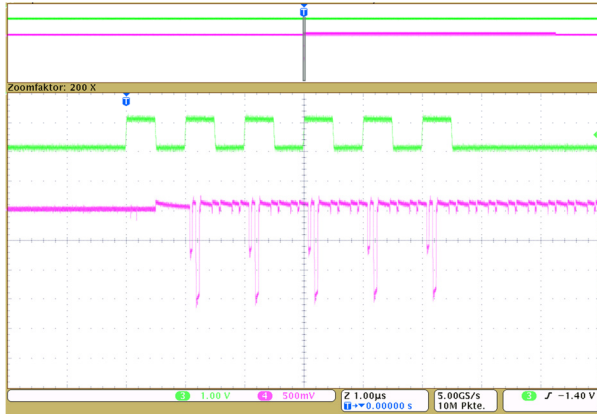


Figure 5: analog signal of x plane at digitizer input with leading initial bunch pulses acquired at AT-mode for same bunch train as shown in Figure 2, (green = bunch trigger (pos. slope); violet = x; y signal not shown).

DESIGN FLEXIBILITY

The LCBPM electronics has been designed for different setups, typically found at different positions along the new FLASH2 accelerator. Specific design adaptations may also enable the use at other accelerators like XFEL and accelerator transfer lines. Operational flexibility covered by the LCBPM design includes

- compatibility to the XFEL accelerator timing system ([3])
- adjustable BPM parameter set (transverse offsets, monitor constants, delayline attenuation factors, digital signal processing etc.)
- 3 / 4.5 MHz bunch-rep-rates + sub-harmonic rates
- 10 / 25Hz macropulse rep-rates + sub-harmonic rates
- single shot (macropulse) ability (event-driven)
- single bunch measurement (first bunch in AT-mode used for triggering – true first bunch AT-mode currently under development)
- relative charge measurement from button sum signal precautions for AGC scheme foreseen at design
- internal test-pulse generator sufficient for self-test and basic BPM channel calibration
- a triggerable external test-pulse-generator is foreseen as an extended performance calibration source inside an LCBPM crate as shown in Figure 1.
- 45° and 90° BPM chamber orientation-modes
- e- and e+ input signal polarity modes (e+ mode requires adaption of RF-frontend)
- 3 enhanced raw-data modes for remote adjustment and input signal investigation purposes

- low-latency-link interface planned for fast feedback purposes
- adjustable bunch orbit alarm detection and maskable low-latency alarm signal generation to MPS
- selectable ADC input data streams for optimum input signal integrity
- enhanced BPM system error detection and status monitoring (Q-value, input data errors, logic errors, trigger state etc.).

COMMISSIONING TESTS AND CONCLUSION

The tests at dedicated test setups show promising performance results. First LCBPM systems have been tested parasitically with beam at FLASH. Recent commissioning tests at FLASH2 have shown stable BPM performance at certain locations. Increased input noise levels were recently found during commissioning at some BPMs at FLASH2. Frontend noise-sources and -distribution as well as algorithms for increased trigger- and signal conditioning stability are under investigation and test for further improvement.

OUTLOOK

Further commissioning tests and performance measurements have to be done with beam at FLASH and FLASH2 for detailed investigation of full functionality and performance. Based on the update of the MicroTCA infrastructure & interface firmware library, the interface to the timing system will be further expanded, to enable section-wise LCBPM pre-conditioning for FLASH2/FLASH bunch trains.

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