# **Progress in Photonic Analog-to-Digital Conversion**

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## (Invited Paper)

Abstract: Recent progress in using photonics for highly-accurate analog-to-digital conversion of wideband RF signals is reviewed, its capabilities and limitations are discussed. A down-converting electronic-photonic ADC digitizing a 41GHz tone with 16fs equivalent jitter is presented. © 2013 Optical Society of America

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#### 1. Introduction

With several decades of research in photonic analog-to-digital converters (ADCs) [1, 2], last few years have seen a renewed interest in this technology [3-7], considered as capable of delivering orders-of-magnitude improvement in accurate digitization of high-speed RF signals. The progress in electronic ADC performance is facing two major challenges: aperture jitter of the sampling clock and comparator ambiguity [8]. In the photonic approach, the problem of aperture jitter is addressed by sampling the RF signal optically with ultra-stable pulse trains available from mode-locked lasers; the timing jitter of such pulse trains can approach few attoseconds [9-12], which is over four orders of magnitude less than the jitter in state-of-the-art electronic ADCs [8]. The second challenge – comparator ambiguity – is completely eliminated by separating the fast RF signal into multiple slower channels, using a time- [13] or a wavelength-demultiplexing [14-16] scheme. With the photonic time-stretch approach [17], the bandwidth of the time-division multiplexed channels is reduced, enabling sampling rates as high as 10 TSa/s [18]. Some recent photonic ADC demonstrations include sampling of a 733 MHz RF tone with 9.8 effective number of bits (ENOB) [19], a 35 GHz tone with 2.5 ENOB [3], 4 GHz with 7.2 ENOB and 10 GHz with 6.65 ENOB [4], 6.5 GHz with 6.65 ENOB and 10 GHz with 6.15 ENOB [5], 40 GHz with 6.0 ENOB [6], and 41 GHz with 7.0 ENOB [7]. What makes these developments especially exciting is that with the recent progress made in silicon photonic and electronic-photonic integration technologies [20-22], it becomes feasible to transfer the photonic ADC systems from an optical table to a single silicon chip. This means that the road is now open to the arrival of an accurate, high-speed, integrated electronic-photonic ADC as a practical consumer product.

In this presentation, we will overview recent progress made in photonic ADCs, explain the principles and main schemes for photonic analog-to-digital (A/D) conversion, present some of our results on the way to build a monolithic photonic ADC, and speculate about the future of photonic ADC technology.

## 2. Principles of Photonic Analog to Digital Converters

After three decades of research, several schemes for photonic A/D conversion have been developed [2]; in the following, we will discuss the scheme we used in our research [7]. Our scheme shares many common features with other principal schemes; a more complete overview of the field will be given in our presentation.

The layout of the photonic ADC investigated here is presented in Fig. 1a. A mode-locked laser, that may or may not be integrated, generates an ultra-low-jitter optical pulse train with repetition period T. This train is split into N trains at different center wavelengths with a wavelength demultiplexer, which are passed through a set of delay lines which introduce incremental time delays of T/N between them. The trains are then recombined into a single path, forming a train of pulses at N-fold primary repetition rate and chirped center wavelength repeating periodically every N pulses [15, 16]. This pulse train passes an electrooptic modulator with the RF signal to be sampled applied to its input; at the output, the energies of the modulated pulses represent the samples of the RF signal taken at the corresponding sampling times. With this approach to sampling, the aperture jitter is determined by the timing jitter of the mode-locked lasers, which can be extremely low [11], thus eliminating the problem of aperture jitter. The modulated pulse train is then taken apart into N wavelength channels. Each of these channels is detected with a photodetector, amplified, and digitized with an electronic ADC which is triggered by the mode-locked laser itself and takes exactly one sample per pulse. Note, although for simplicity we call this ADC a photonic ADC, in reality it is a photonic sampling and electronic quantizing ADC, with electronics performing the critical function of digitizing the modulated pulses, which electronics can do best at high resolutions. At the post-processing stage, the samples captured in different wavelength channels are interleaved and distortion-compensated to obtain the final digital representation of the RF signal. Note, that the scheme with N channels reduces the required analog bandwidth of photodetectors and electronic ADCs in proportion to N, which means that the comparator ambiguity – a major limiting factor at high frequencies [8] – becomes a non-issue.



Figure 1. (a) Layout of the photonic ADC studied here; the components inside the dashed box can in principle be integrated on a single chip; (b) a vision for the photonic ADC implemented as a single electronic-photonic silicon chip [7].

A major advantage of the A/D scheme described above is that the latest developments in silicon photonics and electronic-photonic integration technology make it possible to integrate the whole A/D system on a silicon chip (Fig. 1b). The wavelength multiplexers and demultiplexers can be implemented as banks of microring resonator filters; electrooptic modulators can be implemented as carrier-depletion Mach-Zehnder silicon modulators; germanium photodetectors can be used to convert the modulated pulse trains from the optical into the electrical domain. It is expected that the continuing progress in electronic-photonic integration technology will make it possible to implement the RF amplifiers and electronic ADCs on the same chip with photonic compoments. Such single-chip integration promises to eliminate interconnect parasitics, improve the power efficiency and ADC accuracy. The only component which might yet be difficult to implement on the same silicon chip (although efforts to do so are underway in the DARPA ESPIOR program) is the mode-locked laser; a separate chip, containing an integrated erbium-doped mode-locked planar waveguide laser [23], can be used as a compact optical pulse source.

### 3. Photonic ADC Experiments

The capabilities of the photonic A/D system described above have been explored in the DARPA-EPIC Program jointly by MIT and MIT Lincoln Laboratory. We created two versions of such a sampling system, one with discrete off-the-shelf components, and the other with the core photonic components fabricated on a silicon chip (Fig 2a) [7].

A custom-built mode-locked Er-fiber laser with repetition rate of 1.05 GHz was used as the optical pulse source. Two wavelength channels were implemented in both versions, resulting in an aggregate sampling rate of 2.1 GSa/s. Note that higher sampling rates can be achieved by adding more channels similar to the ones demonstrated here, without changing other parameters of the system.



Figure 2. (a) Photograph of a silicon photonic chip with the core photonic components of the ADC; (b) spectrum of a 41GHz signal captured with a discrete-component version of the ADC; (c) spectrum of a 10GHz signal captured with the silicon chip-based ADC [7]. Signal frequencies were aliased because the number of wavelength channels was less than needed for Nyquist sampling.

The discrete-component ADC system was able to digitize a 41 GHz input tone with 7.0 effective bits (Fig. 2b); offset and gain mismatch between the two channels were compensated at the post-processing stage to eliminate interleaving spurs. This level of performance corresponds to 16 fs equivalent timing jitter, which exceeds the performance of the best electronic ADCs 5-10 times. The accuracy was limited by the noise of the RF amplifiers; it is expected that the accuracy can be improved with further optimization of post-detection electronics.

In a second version, an integrated silicon photonic chip containing the photonic core of the A/D conversion system has been fabricated [24, 7]. The chip contained a carrier-depletion Mach-Zehnder modulator, microring resonator filters for wavelength demultiplexing, as well as all-silicon defect-based photodetectors; discrete components were used to amplify and digitize the RF pulse trains at the outputs of the chip. An accuracy of 3.5 ENOB was achieved for a 10 GHz input tone (Fig. 2c); the accuracy is reduced as compared to the discrete-component system because of the low level of RF signal at the input of the electrical ADCs. This was the result of excess optical losses due to damaged fiber-to-chip couplers, as well as relatively low efficiency on-chip silicon defect-photodetectors (0.1A/W). It is expected that photodetectors with improved performance, such as germanium photodetectors [25] which exhibit efficiencies close to 1 A/W, will significantly improve the ENOB.

#### 4. Discussion

Recent results achieved in photonic ADC demonstrations suggest that the photonic sampling is capable of strongly reducing the role of the two fundamental limitations in ADCs: aperture jitter and comparator ambiguity. This opens up a path to increased speed and resolution in A/D conversion. If the currently observed low levels of timing jitter in mode-locked lasers can be translated into effective bits, one will be able to digitize signals of up to THz bandwidth with more than 10 ENOB. Together with silicon photonics as the integration platform finally a practical, cheap, integrated solution for photonic ADCs has arrived, that might surpass its completely electronic counterpart by potentially more than three orders of magnitude in achievable resolution spectral detection, therefore boosting the spectral efficiency of long haul optical transport systems. In electronic warfare dramatic advances in terms of size, weight, power, and cost for communication and multisensor command and control technology seem possible, while boosting the performance of these systems by orders of magnitude.

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