Photonic ADC: overcoming the bottleneck of electronic jitter

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Abstract: Accurate conversion of wideband multi-GHz analog signals into the digital domain has long been a target of analog-to-digital converter (ADC) developers, driven by applications in radar systems, software radio, medical imaging, and communication systems. Aperture jitter has been a major bottleneck on the way towards higher speeds and better accuracy. Photonic ADCs, which perform sampling using ultra-stable optical pulse trains generated by mode-locked lasers, have been investigated for many years as a promising approach to overcome the jitter problem and bring ADC performance to new levels. This work demonstrates that the photonic approach can deliver on its promise by digitizing a 41 GHz signal with 7.0 effective bits using a photonic ADC built from discrete components. This accuracy corresponds to a timing jitter of 15 fs – a 4-5 times improvement over the performance of the best electronic ADCs which exist today. On the way towards an integrated photonic ADC, a silicon photonic chip with core photonic components was fabricated and used to digitize a 10 GHz signal with 3.5 effective bits. In these experiments, two wavelength channels were implemented, providing the overall sampling rate of 2.1 GSa/s. To show that photonic ADCs with larger channel counts are possible, a dual 20-channel silicon filter bank has been demonstrated.

OCIS codes: (060.5625) Radio frequency photonics; (070.1170) Analog optical signal processing; (320.7085) Ultrafast information processing.

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1. Introduction

The field of electronic data conversion has witnessed significant progress over the last decade. With the unity gain frequency of CMOS technology reaching hundreds of gigahertz and matured SiGe technology, data converters based on the silicon platform operating at sampling rates of tens of GSa/s now exist. For instance, Fujitsu Inc. recently introduced a 65 GSa/s ADC in CMOS [1]. Prior to that, Nortel Inc. had demonstrated a 40 GSa/s CMOS ADC [2], and Rensselaer Polytechnic Institute had introduced its 40 GSa/s SiGe ADC [3]. While radio frequency (RF) electronic data converters are now running at unprecedented sampling rates, their performance, as defined by effective number of bits (ENOB), has not improved commensurately. A major factor limiting the progress towards higher rates and resolutions is aperture jitter, i.e. inability of ADCs to sample at precisely defined times. Figure 1 shows ENOB as a function of input frequency for high-performance electronic ADCs, as reviewed by Walden [4], including some ADCs that have appeared afterwards. Dashed lines represent limits on ENOB due to jitter. The best electronic ADCs deliver jitter levels of 60-80 fs in the 100-400 MHz frequency range; reducing the jitter further becomes increasingly difficult, especially beyond gigahertz frequencies, and if the past is a good prediction for the future, it will take nearly a decade to improve the jitter performance by an order of magnitude [4]. As discussed below, ultra-stable mode-locked laser sources with jitter levels many orders of magnitude lower exist today; if used for sampling, they could improve ADC performance by orders of magnitude.

In this work, the potential of the photonic approach is demonstrated by sampling a 41 GHz signal with record 7.0 ENOB with a discrete-component photonic ADC. This performance is equivalent to 15 fs jitter, a significant improvement over today's state-of-the-art. A practical photonic ADC must be integrated on a chip, which can be realized using rapidly developing silicon photonics technology. A chip incorporating the core optical components of the photonic ADC (a modulator, wavelength demultiplexers, and photodetectors) has been fabricated and shown to produce 3.5 ENOB for a 10 GHz input. The above experiments were performed using two 1.05 GSa/s wavelength channels, with the aggregate sampling rate of 2.1

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GSa/s. A 20-channel filter bank was demonstrated as a key component for enabling photonic ADCs with increased number of channels and higher sampling rates. The obtained results indicate that fast and accurate photonic ADCs can be realized today and suggest that even better results can be achieved in the future through the synergistic integration of electronics, silicon photonics, and ultra-stable mode-locked laser technologies.

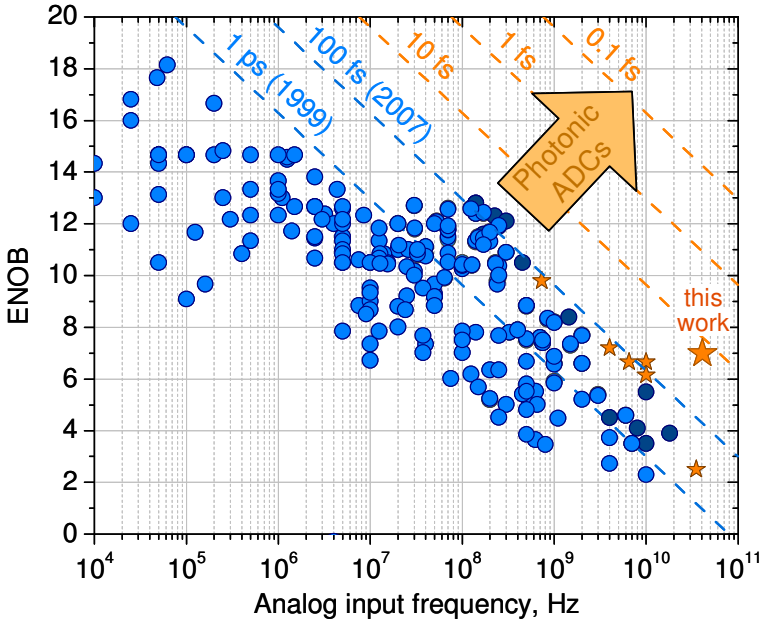

Fig. 1. "Walden plot" showing ENOB of existing ADCs as a function of analog input frequency. Each point represents an ADC: blue circles correspond to the ADCs from Walden's survey of ADCs as of late 2007 [4], and dark blue circles correspond to some high-performance ADCs that have been demonstrated since 2007. The dashed lines are locii of constant values of aperture jitter, as indicated next to the lines together with the year when this jitter value was achieved. Photonic ADCs, operating with very low timing jitter, are envisaged to bring ADC performance to new levels, as indicated by the arrow labeled "Photonic ADCs". Some high-performance wideband photonic ADC results are shown with orange stars, with the large star corresponding to the result of this work. Note that all photonic ADC results in this plot, including the result of this work, were obtained in the undersampling mode, i.e. when signals were sampled below their Nyquist rates. Details on data points used in this plot can be found in the Appendix.

2. Timing jitter of RF and photonic sources

Today's electronic data converters derive their sampling clock from RF oscillators. The timing jitter or phase noise of these oscillators is governed by the laws of thermodynamics and therefore is fundamentally limited by the thermal noise of the resonator and active elements of the oscillator, which sets stringent limits at room temperature operation. Whatever the noise source is, the addition of random noise to a sinusoidal signal of given amplitude leads to an uncertainty of the zero crossing proportional to the signal period. Higher frequency oscillators will therefore show lower timing jitter than a lower frequency oscillator with otherwise identical components and noise [5]. Specifically, for ultrashort laser pulses whose microwave phase undergoes a random walk in the laser cavity due to spontaneous emission noise, the standard deviation Δt of the center of gravity of pulses from their nominal positions grows in time according to a diffusion law [6] and scales with the measurement time T_M as $\Delta t \sim \tau\sqrt{h\nu T_M / E_P \tau_c}$, where τ is the pulse duration, E_P the intracavity pulse energy, τ_c the cavity decay time and $h\nu$ the photon energy. Thus mode-

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locked lasers producing 10-100 fs optical pulses can serve as sampling clocks that can be 10^3 to 10^4 times lower in jitter compared to their microwave driven counterparts with a typical period of 100 ps and otherwise similar parameters. Note that ultra-high Q microwave oscillators, such as sapphire loaded cavity resonators (eventually even cryogenically cooled) or opto-electronic delay line oscillators, can deliver very low jitter, but at a significantly higher cost and size.

Experimental verification of the low timing jitter of mode-locked lasers started as early as 1986 [7–10]. Optical techniques for timing jitter measurements, such as the recently introduced balanced optical cross-correlation technique [5], confirmed that passively mode-locked lasers show jitter levels of less than 3 fs for standard fiber lasers [11,12] and about 10 as for solid-state lasers due to their shorter pulses, higher intracavity pulse energy and lower intracavity loss [13]. In fact, this latter value is the lowest jitter or phase noise level ever observed in any oscillator. Some of these sources can even be integrated on a chip [14]. The microwave phase noise at low frequencies or slow drift of the repetition rate, although present in free-running mode-locked lasers, can be suppressed using standard long-term stable frequency references or ultrastable high Q cavities [15–17]. However, for ADC applications, this drift is not crucial since it can be measured and compensated for during post-processing. Note that the low timing jitter or microwave phase noise has also been explored in the past in different mode-locked laser platforms [18,19].

This jitter scaling from microwave to optical sources, together with rapid progress in electronic-photonic integration via the silicon photonics technology platform, gives confidence that the 3-4 orders of magnitude in jitter reduction, possible with mode-locked lasers, can be exploited to bring ADC performance to levels well beyond what is possible today. The potential for improvement is significant: the reduced jitter level expands the region of possible sampling speed-resolution products to beyond the 100-as boundary in Fig. 1. This means that if these low jitter values could be exploited to realize a jitter-limited ADC, this would revolutionize processing of signals potentially up to THz bandwidths with more than 10 ENOB. Of course, there are many practical problems apart from the jitter which need to be solved before such performance levels can be approached.

3. Photonic analog-to-digital converters

To overcome the aperture jitter in the sampling process, photonic ADCs perform sampling in the optical domain using low-jitter optical pulse trains. Sampling occurs when such pulse trains pass through an electro-optic modulator while the voltage signal to be sampled is applied [20]; the output pulse energies represent the RF signal values at the temporal positions of the pulses. A major benefit of this approach is that the jitter of the optical sampling process is determined by the jitter of the optical pulse train, which, as explained above, can be extremely low. Another benefit is that electro-optical interactions are very fast; the aperture over which the RF signal is sampled, as defined by the duration of optical pulses, can be very short. Moreover, to handle the enormous data flow generated when sampling high frequency signals, photonic approaches offer the possibility to split the input into multiple lower-rate channels to be processed in parallel, as described below.

The ADC architecture used in this work is illustrated in Fig. 2. In an N-channel ADC, an optical pulse train with repetition period T is split into N trains, each centered at a different wavelength, with a 1-to-N wavelength demultiplexer. These trains pass through optical delay lines, which introduce incremental delays of T/N between them. The trains are then recombined with a multiplexer to produce a pulse train with repetition period T/N, where pulse wavelengths repeat periodically every N pulses. This operation establishes a discrete time-to-wavelength mapping within the pulse train, i.e. pulses separated in time are also separated in wavelength [21,22]. A continuous version of time-to-wavelength mapping can be established with a dispersive fiber [23,24]. The next step is the optical sampling, i.e. modulation of the optical pulse train with the RF signal to be sampled [20]. The modulated pulse train is then taken apart into N channels using a wavelength demultiplexer matched to the one used earlier to establish the time-to-wavelength mapping. The pulse trains in all

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channels are converted to the electrical domain with photodetectors, boosted in amplitude with RF amplifiers, and digitized with electronic ADCs. These ADCs are synchronized with the mode-locked laser and take one sample per pulse, exactly at the pulse peak. Although the electronic ADCs have some aperture jitter, the accuracy of the photonic ADC is insensitive to it because the electronic ADCs sample the relatively flat-top region of the pulses. During post-processing, the samples captured in different channels are compensated for distortions and interleaved to obtain the final digital representation of the RF signal. Note that the scheme with N channels not only increases the sample rate by N, but also reduces the required analog bandwidth of photodetectors and electronic ADCs [24], which need to be only as high as several times the original laser repetition rate to avoid intersymbol interference between subsequent pulses. Importantly, because of reduced analog bandwidth at the input of electronic ADCs, the impact of comparator ambiguity – another major factor limiting accuracy at high frequencies [4] – is completely eliminated.

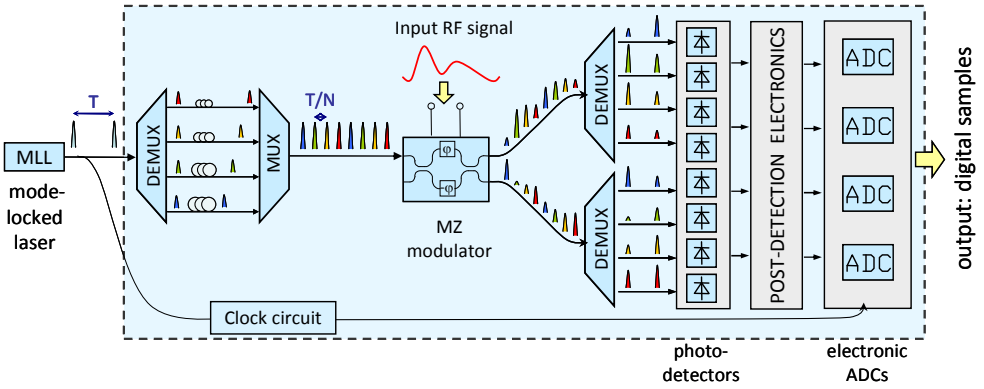

Fig. 2. Layout of the photonic ADC studied in this work. The components of the ADC inside the dashed box can ultimately be integrated on a single electronic-photonic chip. In this work, the silicon chip comprised the modulator, demultiplexers, and photodetectors, while all other components were implemented off-chip, as described later.

Photonic ADCs have been actively investigated over the last decades; an overview and classification of photonic ADCs can be found in an excellent review by Valley [25]. The idea of optical sampling originates from the works of Taylor et al. [20]. Wavelength-demultiplexing scheme was proposed by Frankel et al. [24], preceded by a work of Valdmanis, who discussed a similar concept to improve time resolution of oscilloscopes [23]. Wavelength-demultiplexing based on discrete time-to-wavelength mapping – the approach adopted in this work – was proposed by Yariv [21] and Kang [22]. A time-demultiplexing approach [26] was adopted by Juodawlkis et al. [27], who analyzed the performance of optically-demultiplexed ADCs and developed calibration techniques which helped to demonstrate 9.8 ENOB for a 733 MHz signal sampled at 505 MSa/s in an 8-channel system in a work by Williamson et al. [28]. A prominent way to increase ADC speed is the photonic time-stretch approach pioneered by the group of Jalali [29]. In this approach, one fiber introduces continuous time-to-wavelength mapping at the input of the modulator, and another fiber further stretches the modulated signals to slow them down and enable high-speed sampling [29,30]. A short-pulse digitizer operating at astonishing 10 TSa/s with 4.5 ENOB has been demonstrated with this approach [31]. On the way to achieving continuous time operation, 6-7 effective bits were recently reported over a 10 GHz bandwidth by the group of Valley [32], 6.7-7.2 effective bits were obtained over a 10 GHz bandwidth by the group of Jalali [33], and 2.5 bits were reported for a 35 GHz input sampled at 150 GSa/s [34]. Sophisticated calibration of time-stretch ADCs was applied to achieve these results [32–34]. Other impressive results include 8.0 ENOB at 10 GHz [35] and 7.0 ENOB at 40 GHz [36], achieved in narrowband optically-sampled ADCs. The systems described above use electronic quantization. Another class of ADCs performs quantization optically [20,25,37–39]; many

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promising schemes have been demonstrated, and efforts are in progress to improve their accuracy beyond a few bits.

4. Demonstration of a discrete-component photonic ADC

To demonstrate low-jitter sampling of high-frequency signals, a photonic ADC based on the concept described above (Fig. 2) was built using discrete commercially available components. This section describes the implementation of this photonic ADC with two 1.05 GSa/s channels interleaved to provide 2.1 GSa/s aggregate sampling rate, and presents results of digitization of a 41 GHz test signal.

The photonic ADC testbed was built with the following commercially available discrete components. To create a wavelength-interleaved pulse train, a standard fiber-coupled 1:8 thin-film wavelength demultiplexer (JDSU, DWM-2F8DS, 200 GHz channel spacing, 150 GHz bandwidth), as well as variable delay lines (Santec, ODL-330), were used. Two wavelength channels were implemented; with 1.05 GHz repetition rate of the laser, the aggregate sampling rate was 2.1 GSa/s. The wavelength-interleaved pulse train was amplified by an EDFA (MPB R35/130), providing 40 dB of gain. A test RF signal was generated with an RF synthesizer (Anritsu 69077B), amplified with an RF amplifier (SHF 803), and passed through a bandpass filter (Wiltron W-band BPF, 33-50 GHz) which rejected undersired frequencies from the input signal.

The modulator was a dual-output $LiNbO_3$ Mach-Zehnder modulator (EOSpace, model AZ-1x2-AV5-40-PFA-SFA); its 3 dB bandwidth, which determined the analog bandwidth of the whole photonic ADC, was approximately 40 GHz. The modulation depth was about 23%. To demultiplex the pulse trains at the two outputs of the modulator, thin-film wavelength demultiplexers of the same mode were used (JDSU, DWM-2F8DS). The optical signal was detected with 40 GHz balanced photoreceivers (U2T Photonics, BPRV2125). Differential detection increased SNR by 3 dB, rejected common mode noise, canceled quadratic nonlinearity, and created a signal which spans both positive and negative voltage values to match the input voltage range of electronic ADCs. To boost the detected signal to the 1.0 V peak-to-peak input voltage of electronic ADCs, a post-detection electronic link was used, consisting of a 3 GHz Gaussian low-pass filter, a DC block, a preamplifier (H2 Com 24471, 19-dB gain), another DC block, an amplifier (Hittite 641, 13-dB gain), and a balun. The electronic ADCs (National Semiconductor, ADC10D1000) had two 1 GSa/s differential input channels operating at approximately 9.0 ENOB and were preconfigured on an evaluation board with a Virtex 5 FPGA. The ADCs were synchronously clocked with an RF signal regenerated from the unmodulated optical pulse train using an amplified photodiode, RF filter, and clock distribution circuit (National Semiconductor, LMK01000). Variable optical and RF delay lines were used to precisely align the modulated pulse train with the ADC sampling clock to ensure that pulses are sampled at their peaks.

The only custom-built component used in the experiments was the low-jitter mode-locked laser, which was a soliton mode-locked Er-doped fiber laser, self-starting with a semiconductor saturable Bragg reflector [40]. The linear laser cavity consisted of a 93-mm long erbium-doped gain fiber (Liekki Er80-8/125) that was spliced to a 7-mm long piece of standard single mode fiber (SMF-28e) to prevent thermal damage of the butt-coupled saturable Bragg reflector. With 10% output coupling, 10 mW of output power was obtained for an optical spectrum centered at 1560 nm with a 10 nm 3-dB bandwidth at a fundamental repetition rate of 1.05 GHz (more precisely, 1.048 GHz). In experiments with the silicon photonic chip described below, the laser cavity was adjusted to shift the center wavelength close to 1572 nm with a 3-dB bandwidth about 13 nm in order to match the resonances of the microring filters. The integrated timing jitter for the free-running laser, extracted from a single-side band phase noise measurement with a signal source analyzer, was determined to be about 13.8 fs within [10 kHz...10 MHz] frequency interval and 10.8 fs within [100 kHz...10 MHz] interval [40]. These values are the upper limit for the timing jitter of the laser since the noise floor of the signal source analyzer contributes to the phase noise measurement experiments; the real jitter of the laser can be lower.

#156800 - $15.00 USD Received 19 Oct 2011; revised 1 Feb 2012; accepted 1 Feb 2012; published 8 Feb 2012

The ADC was tested by digitizing a single-tone 41 GHz signal. Spectra of the data points captured in two channels are shown in Fig. 3(a); these spectra are the Fourier transforms of the raw unprocessed data, only with Blackman windowing function applied to improve the dynamic range. These data points were interleaved and post-processed offline on a computer. Despite careful adjustment of the delay values, some amount of timing skew between the channels was observed; the timing skew was digitally compensated by finding numerically the amount of timing offset which would minimize spurious frequency components in the interleaved data. Gain and offset mismatch between the two channels were digitally compensated as well. The gain mismatch was found from the condition that peak-to-peak amplitude in both channels must be the same. The offset mismatch was found by minimizing the interleaving spurs. The nonlinearity of the sinusoidal transfer function of the MZ modulator was compensated by taking arcsine [41,42] of the data points multiplied by a factor which was determined so as to minimize harmonic distortions in the resulting data. Improvement of spurious-free dynamic range (SFDR) due to linearization was about 5 dB for the 41 GHz RF input. Note that the timing and gain errors observed for the photonic ADC are also common to multi-channel electronic ADCs. To compensate for these errors as well as for the nonlinearity of the modulator, a practical photonic ADC can use one of the multiple calibration and compensation algorithms successfully applied in modern electronic ADCs. Compensation algorithms developed for photonics ADCs can be used as well [28,32,33]. Finally, note that the main conclusion of this work is that the photonic approach can overcome the electronic timing jitter, which manifests itself as the noise floor. The data processing described above changed only harmonic distortions, but not the noise floor, therefore this conclusion holds regardless of the data processing applied.

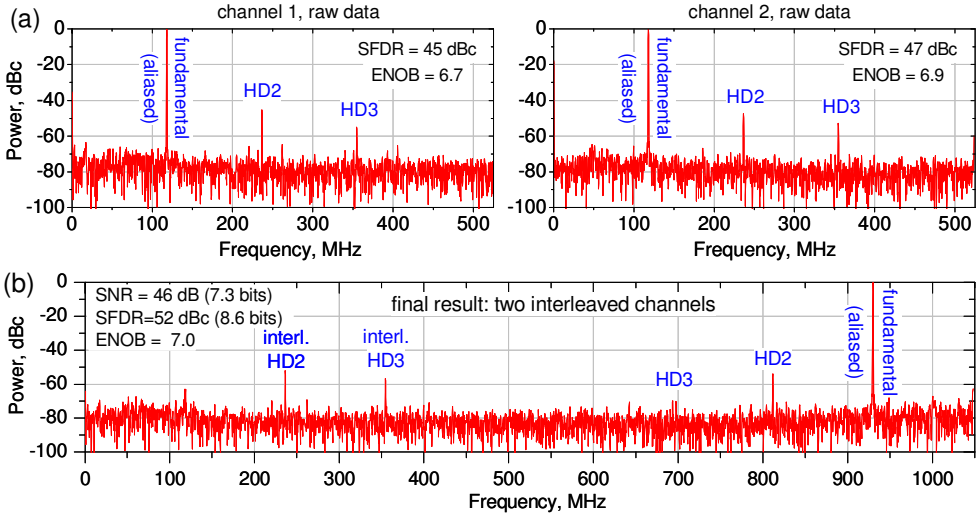

Fig. 3. Data measured with two 1.05 GSa/s channels of the discrete-component photonic ADC. This ADC was used to digitize a 41 GHz RF signal. Fourier transforms of the data points recorded in individual channels are shown in (a), and Fourier transform of interleaved data is shown in (b). Since the sample rate per channel (precise value 1.048 GSa/s) was lower than the Nyquist rate for the test signal (precise frequency 40.99 GHz) signal, the signal was aliased to 118 MHz in (a) and 930 MHz in (b). The signal at fundamental frequency is labeled as "fundamental", second and third harmonic distortions are labeled as "HD2" and "HD3", and interleaving spurs are labeled as "interl. HD2" and "interl. HD3". 4096 data points were captured in each channel; a Blackman window was applied to improve the dynamic range.

Figure 3(b) shows the final result – the spectrum of the 41 GHz RF signal sampled at 2.1 GSa/s with 7.0 ENOB and 52 dBc SFDR. This significantly exceeds any result achieved with electronic ADCs at such high frequencies (see Fig. 1). Such performance corresponds to the aperture jitter of 15 fs or smaller – a 4-5 times improvement over the jitter of the best

#156800 - $15.00 USD Received 19 Oct 2011; revised 1 Feb 2012; accepted 1 Feb 2012; published 8 Feb 2012

electronic ADCs and about an order of magnitude improvement over electronic ADCs operating at frequencies above 10 GHz.

It is necessary to emphasize that apart from the timing jitter, other factors can also contribute to the noise floor of the photonic ADC, such as the thermal and shot noise of photodetectors, RF amplifier noise, electronic ADC noise, as well as the amplitude noise of the mode-locked laser. The 15 fs jitter level quoted above corresponds to the equivalent jitter, i.e. the amount of jitter which would limit the SNR to the observed level in absence of all other noise sources. In fact, in the present experiments, the jitter was not the main limiting factor, because it was observed that in the absence of optical input the RF subsystem generated a noise floor which was only 1-2 dB below the noise floor shown in Fig. 3, i.e. the RF amplifier noise was the limiting factor. The 15 fs equivalent jitter quoted above provides the upper ceiling for the jitter value, i.e. the actual jitter in the present experiments was at most 15 fs (and probably it was lower).

5. Demonstration of a photonic ADC based on an integrated silicon photonic chip

The photonic ADC presented above was made with discrete components in a laboratory setting, similarly to most other photonic ADCs demonstrated to date. However, to be a viable alternative to electronic ADCs, a photonic ADC must be integrated on a chip. Integration enables robustness, miniaturization, potential low-cost mass production, and promises to improve power efficiency and signal integrity by eliminating interconnects between separate chips. A major benefit of the approach pursued in this work is that it allows integration, and a full photonic ADC can potentially be implemented on a single chip using silicon photonics technology, as envisaged in Fig. 4. Such an ADC would use microring-resonator filters, a silicon carrier-depletion modulator [43–45], and germanium [46] or silicon defect-based [47] photodetectors. Post-detection electronics, electronic ADCs, and digital error correction circuits would be integrated on the same CMOS chip. The demultiplexer, time delays, and multiplexer necessary to create a wavelength-interleaved pulse train can also be on the same chip. The pulse train can be generated with a separate chip, for example with an integrated erbium-doped mode-locked planar waveguide laser [14]. This ADC would be an example of a device operating on completely new principles enabled by silicon photonics and electronic-photonic integration.

#156800 - $15.00 USD Received 19 Oct 2011; revised 1 Feb 2012; accepted 1 Feb 2012; published 8 Feb 2012

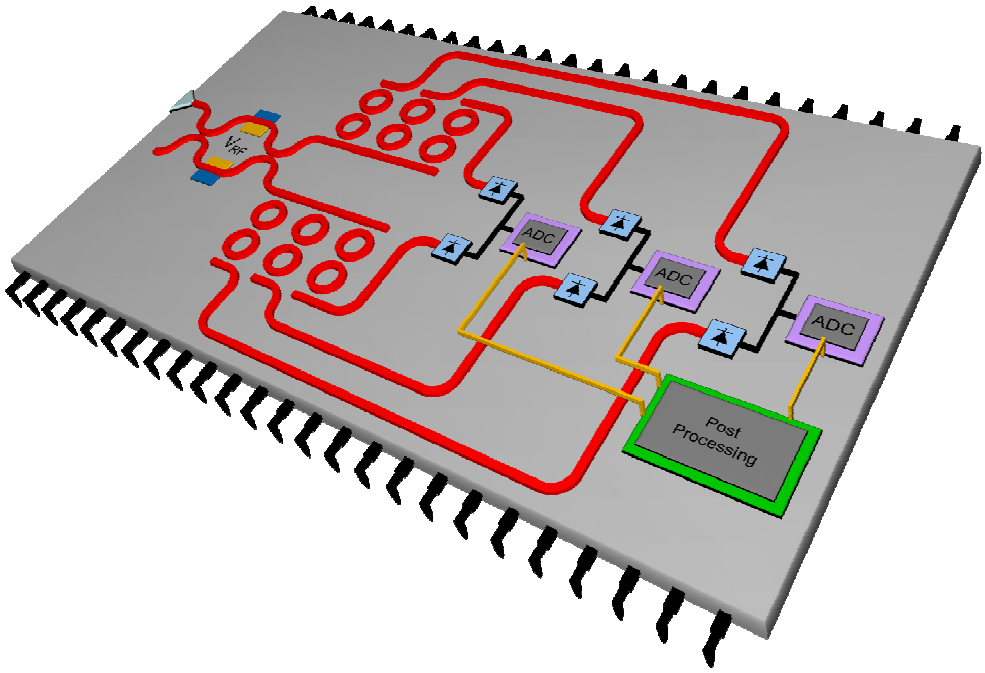

Fig. 4. A vision of a fully integrated electronic-photonic ADC. The chip would include both photonic and electronic components, i.e. a dual-output silicon modulator, two matched banks of microring-resonator filters, balanced photoreceivers, electronic ADCs, and digital post-processing circuits. The generation of the wavelength-interleaved pulse train (not shown in the figure) could also be integrated on the same chip. For simplicity, only 3 wavelength channels are shown; channel count can be significantly higher, as explained later. The silicon chip presented in this work is a first step toward full integration and includes the core photonic components of the ADC (the modulator, filter banks, and photodetectors).

In a move towards a fully-integrated photonic ADC, a chip with core optical components of the above ADC has been created. The chip included a modulator, two matched three-channel filter banks, and photodetectors; the packaged chip is shown in Fig. 5(a), and its top-view photograph is shown in Fig. 5(b). The details of the implementation are given below.

The chip was fabricated on a Unibond silicon wafer with 3 μm buried oxide layer using conventional 248 nm optical lithography. It was overcladded with a 1.0 μm-thick PECVD deposited oxynitride layer (refractive index 1.57).

#156800 - $15.00 USD Received 19 Oct 2011; revised 1 Feb 2012; accepted 1 Feb 2012; published 8 Feb 2012

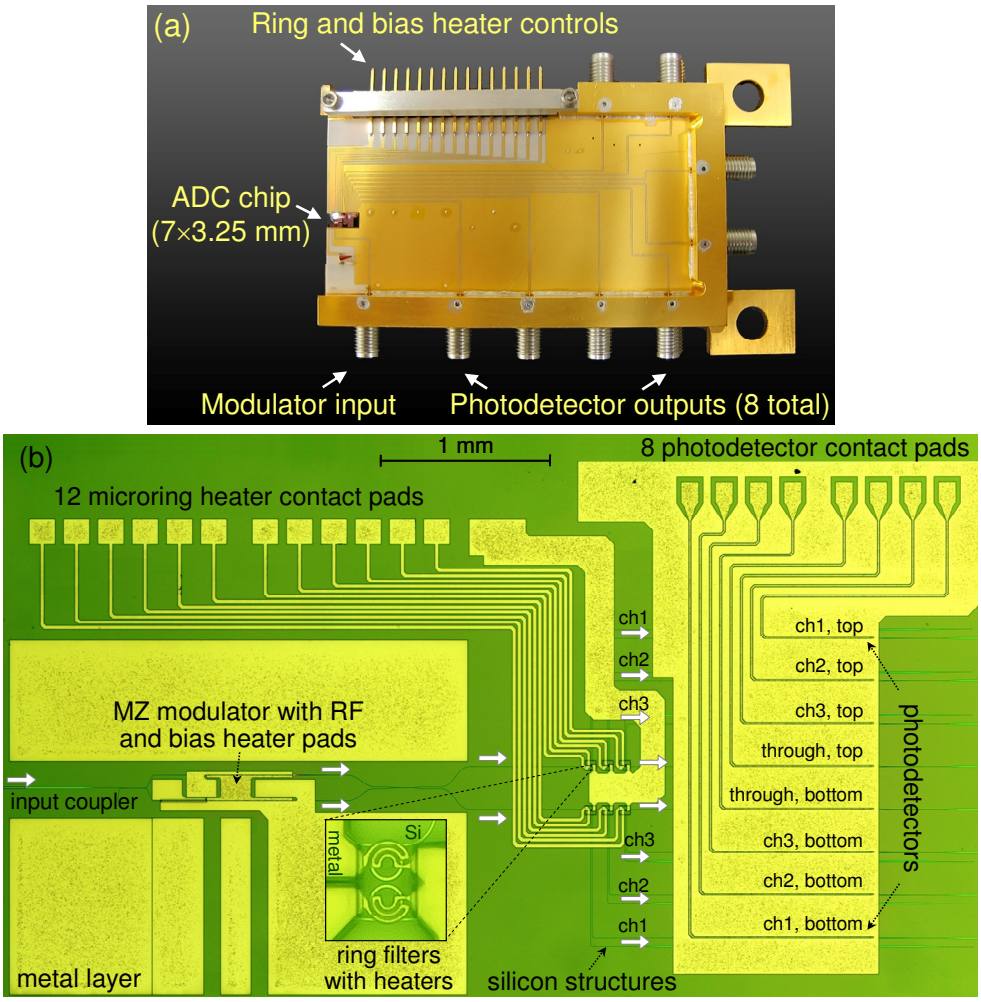

Fig. 5. (a) Photograph of the packaged silicon photonic chip which enables a photonic ADC with three wavelength channels. The chip includes a Mach-Zehnder silicon modulator, two matched three-channel microring-resonator filter banks, silicon photodetectors, and fiber-to-chip couplers. The packaging provides access to 8 RF photodiode outputs (each of the two filter banks has 4 outputs: 3 outputs for 3 wavelength channels and 1 output for off-resonance light, which passes through unaffected by the filters and is used for testing purposes). The package also has DC contacts for microheaters for the filters and MZ modulator. The wavelength-interleaved pulse train generator and all electronic components of the ADC system are implemented off-chip. (b) Top-view photograph of this photonic chip with metal heaters, wiring, and contact pads fabricated on top of the overcladding on the silicon layer.

A fiber-to-chip coupler was used to couple the laser-generated pulse train from a lensed fiber into a sub-micron silicon waveguide. The coupler used a 200 µm-long inverse adiabatic silicon taper [48] inside a fiber-matched oxynitride rib waveguide. The rib was made directly on top of the 1.0 µm-thick oxynitride overcladding and was 3.0 µm wide and 2.0 µm tall. A coupling loss of about 2.0 dB was measured using a lensed fiber with 3.0 µm mode field diameter. The facet was damaged during packaging, increasing the coupling loss to approximately 5 dB.

The electrooptic modulator was a Mach-Zehnder (MZ) modulator with silicon phase shifters in each arm, operated in push-pull mode [44,45]. The phase shifters were implemented as 500-µm-long reversely-biased silicon diodes [43]. The applied RF voltage modulates the distribution of free carriers at the boundaries of the depletion zone; this

#156800 - $15.00 USD Received 19 Oct 2011; revised 1 Feb 2012; accepted 1 Feb 2012; published 8 Feb 2012

modulates the refractive index of silicon via the plasma dispersion effect, and therefore the phase of optical radiation propagating through the diodes. An MZ interferometer converts the phase modulation into an amplitude modulation. In this work [45], two identical 500 μm-long diodes were used in the arms of the MZ structure; the diodes were 500 nm wide and 210 nm thick, doped p-type to $5 \cdot 10^{17}$ cm^{-3} everywhere except 50 nm layers at the top and the right sidewall, where it was doped n-type to $1.5 \cdot 10^{18}$ cm^{-3}, and a 50 nm layer at the left sidewall, where it was doped p-type to $1 \cdot 10^{18}$ cm^{-3}. This design was selected to achieve improved sensitivity in reverse bias, at the expense of some bandwidth compared to previous designs [45]. A microheater fabricated on top of one of the arms was used to thermally adjust the phase difference between the two arms to bias the modulator at quadrature. DC measurements indicated single-arm $V_\pi L = 1.2$ V·cm (or 0.6 V·cm in push-pull configuration), and a 3 dB RF bandwidth was found to be 12 GHz. The insertion loss was approximately 3 dB.

Two matched banks of dual-ring resonator filters, one per modulator output, were implemented for wavelength demultiplexing. The silicon waveguides were 210 nm tall and 360 nm wide. The width of the ring waveguides was larger, 450 nm. The center radius of the rings was 2.32 μm. The coupling gap between the bus and the ring was 225 nm, designed to provide 3.9% power coupling, and the gap between the two rings was 505 nm, designed to provide 0.043% coupling. Titanium microheaters on top of each ring were used to compensate for fabrication variations and place the resonances at desired wavelengths. The microheaters were 1.1 μm above the waveguides, separated from them by an oxinitride overcladding layer; the titanium wires were 500 nm wide and 100 nm thick.

All-silicon photodetectors were used to detect the modulated optical pulses. Absorption at 1.55 μm was induced by ion implanting Si to damage the silicon lattice and create light-absorbing mid-gap states [47]. The implantation (dose = 10^{14} cm^{-2}), followed by anneal (1 min. at 600°C), takes place after activation of all other implants and leaves mid-gap states, which absorb light at around 1550 nm. The efficiency of the 500 μm photodetectors used in the integrated ADC system was about 0.1 A/W. Longer lengths diodes with different implant and anneal conditions have been shown to be more efficient [47], but the exact conditions necessary for this efficiency have been difficult to reproduce. Differential detection was not implemented in the present chip and signals from just one of the two outputs have been used. The bandwidth of the photodetectors was about 3 GHz, enough for detecting 1 GHz pulse trains.

To create smoother sidewalls, and thereby lower the scattering in the waveguides, the resist can be reflowed prior to the etching of the waveguides. After exposure and development, the photoresist (Rohm and Haus, UV5) was baked at 160°C for 5 minutes.

The packaging (Fig. 5(a)) was designed with the chip placed at one edge of the package. Light was edge-coupled into the chip from a fiber lens. A standard printed circuit board contained DC leads for heater and bias control, and also RF waveguides. The RF waveguides were in a Ground-Signal-Ground (G-S-G) co-planer configuration and were used to connect to the modulator and the photodetectors. The RF waveguides met up with K-type connectors at the edge of the package for connecting cables to the package.

The fabricated silicon photonic chip was used for sampling of a 10 GHz RF signal. The testbed was similar to the one used for the discrete component ADC demonstration, except now the heart of the ADC – the modulator, filters, and photodetectors – was on a single silicon chip, as described above. Two out of the available three wavelength channels were used, providing 2.1 GSa/s aggregate sampling rate. Figure 6(a) shows spectra of the data captured in each channel, and Fig. 6(b) shows the spectrum of the interleaved data, with 3.5 ENOB and 39 dBc SFDR.

#156800 - $15.00 USD Received 19 Oct 2011; revised 1 Feb 2012; accepted 1 Feb 2012; published 8 Feb 2012

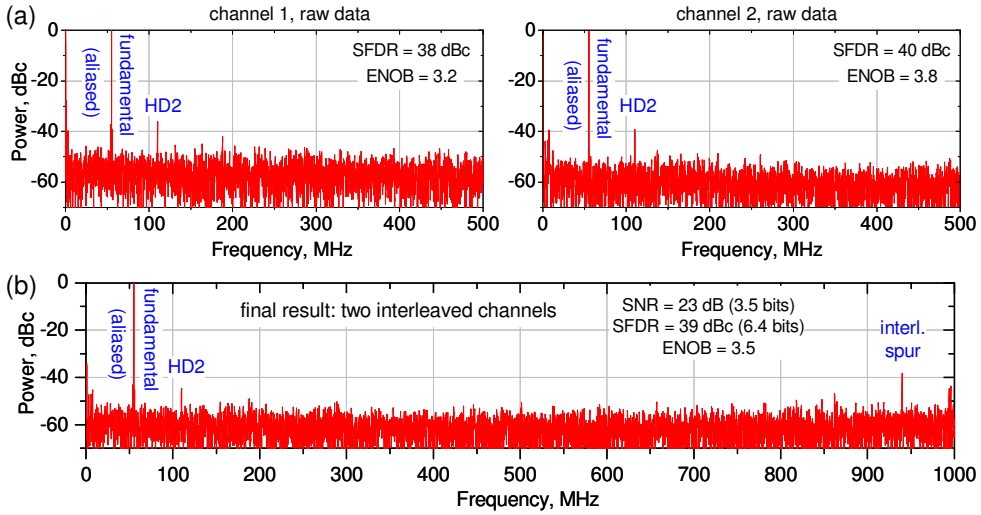

Fig. 6. Data measured with two 1.05 GSa/s channels of the photonic ADC based on an integrated silicon photonic chip. This ADC was used to digitize a 10 GHz RF signal. (a) Fourier transform of data points recorded in individual channels, and (b) Fourier transform of interleaved data. 4096 data points were captured in each channel; Blackman windowing was used to improve the dynamic range.

It is expected that the ENOB, limited by low signal level at the input of the electronic ADCs, can be significantly improved by optimizing the energy efficiency of the chip components, especially the efficiency of silicon photodetectors. Alternatively, highly efficient germanium photodetectors [46] can be used.

Harmonic distortions visible in the spectra of Fig. 6 can be attributed to the silicon MZ modulator. Apart from the sinusoidal nonlinearity of the MZ structure, the nonlinearity of a silicon modulator is affected by the nonlinearity of silicon phase shifters, i.e. the nonlinear dependence of the phase shift in the silicon diodes on the applied voltage. The importance of the phase shifter nonlinearity is in agreement with the fact that, unlike the discrete-component ADC case, taking arcsine of the data did not produce any SFDR improvement (see Fig. 6). In the current version of the chip, the ENOB was limited by low SNR and nonlinear distortions were unimportant, however, once the SNR is improved, the modulator nonlinearity is expected to limit the ENOB. At first glance, significant nonlinearity of silicon phase shifters seems to make a silicon modulator an unlikely candidate for such linearity-sensitive analog applications as photonic ADCs. However, more careful consideration shows that the silicon phase shifter nonlinearity can be cancelled against the sinusoidal MZ nonlinearity for certain combinations of the diode phase shifter length and bias voltage [49]. As a result, it was predicted that the linearity of the silicon MZ modulator can exceed the linearity of a conventional MZ modulator with perfectly linear phase shifters (e.g. a $LiNbO_3$ modulator) [49]. Implementing such a linearized silicon modulator would be an important step towards an accurate integrated photonic ADC. Other modulator linearization techniques [50] and nonlinearity post-compensation can also be used.

6. Scaling to higher sampling rates

While the photonic ADCs described above used two channels and were operated in undersampling mode, the sampling rate can be raised by simply adding more wavelength channels similar to the ones demonstrated above. To show that an ADC with a large number of channels is feasible, a key component of such an ADC – a dual multi-channel filter bank – has been created.

This dual filter bank consisted of two matched 20-channel two-ring filter banks fabricated on a silicon chip, see Fig. 7(a). This dual filter bank was fabricated separately from the

#156800 - $15.00 USD Received 19 Oct 2011; revised 1 Feb 2012; accepted 1 Feb 2012; published 8 Feb 2012

integrated ADC (Section 5) and used a different ring filter design. Microring resonator parameters were as follows: silicon waveguide thickness = 114 nm, width = 495 nm, width of the ring waveguides = 600 nm, ring center radius = 6.735 μm, ring-bus coupling gap = 300 nm (4.7% power coupling), ring-ring gap = 620 nm (0.068% coupling). Refractive index of the oxynitride overcladding was 1.55. The resist reflow step, which was performed to reduce sidewall roughness for the integrated silicon chip (Section 5), was no longer necessary because the thinner waveguides used in the 20-channel filter bank inherently have less scattering, so this step was left out. Titanium microheaters were fabricated 1.2 μm above the waveguides; the wires were 500 nm wide and 300 nm thick. Microheaters on top of each of the 80 rings were used to fine-tune their resonant frequencies with 50 GHz/mW efficiency.

The filter bank was characterized using external photodetectors. For thermal tuning, voltage was applied to the microheaters using electrical probes; only one channel at a time was tuned and measured. The total power to tune all filters was about 400 mW. Figure 7(b) shows the measured transmission of the channels with the 80 GHz spacing. The 32-36 dB suppression of the neighboring channel is sufficient for a 20-channel ADC with ENOB = 10. The total optical bandwidth is about 13 nm, which is easily within the bandwidth of mode-locked lasers at 1550 nm. This demonstrates that all components needed for a photonic ADC sampling at tens of GSa/s are available.

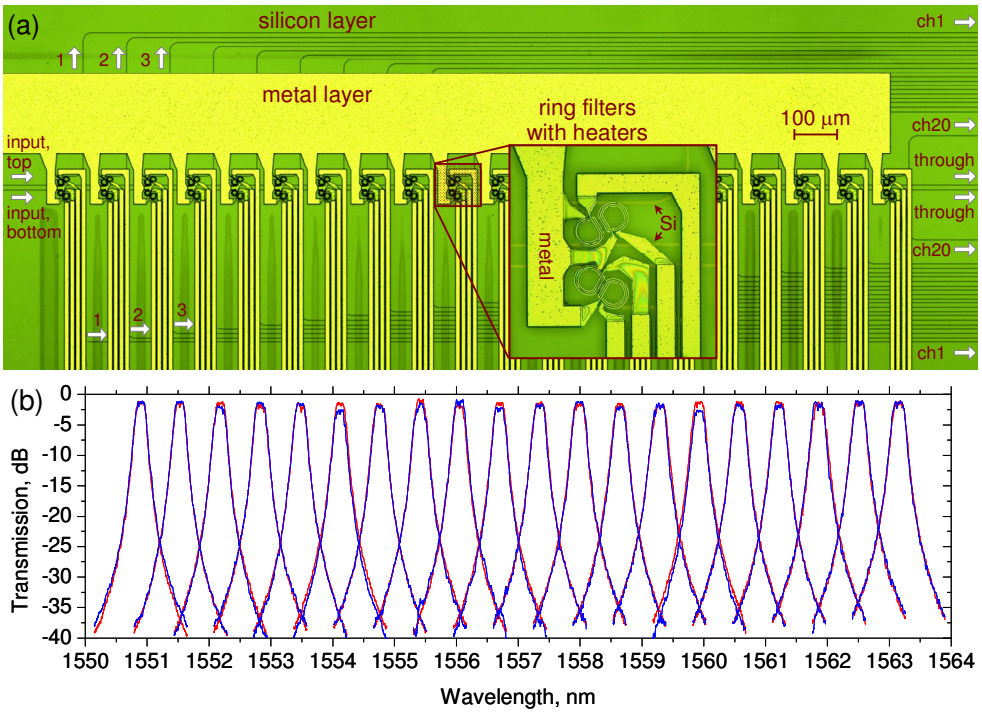

Fig. 7. (a) Photograph of two matched 20-channel filter banks fabricated on a silicon chip. Each bank is intended to demultiplex one of the two complementary outputs of the MZ modulator. The filters are second-order microring-resonator filters. Microheaters fabricated on top of each ring are used to thermally tune resonant frequencies in order to compensate for fabrication errors and put the resonances on a desired grid. (b) Measured transmission of the 20 channels; the overlapping red and the blue lines correspond to the two matched banks. The channels exhibit 21-26 GHz bandwidth, 80 GHz channel spacing, and 32-36 dB extinction at center wavelength of an adjacent channel. The transmission is normalized to the transmission of off-resonance light through the system. The average insertion loss is 1.7 dB; values for individual channels range from 1.1 to 2.8 dB likely due to fiber-to-chip coupling loss variations.

#156800 - $15.00 USD Received 19 Oct 2011; revised 1 Feb 2012; accepted 1 Feb 2012; published 8 Feb 2012

7. Summary and discussion

This work demonstrates the potential of the photonic approach to analog-to-digital conversion by building a discrete-component photonic ADC and using it to sample a 41 GHz RF signal with record 7.0 effective bits and 52 dBc SFDR. The feasibility of a practical photonic ADC is demonstrated by creating an integrated silicon chip with a modulator, filters, and photodetectors and using it to sample a 10 GHz signal with 3.5 effective bits. In both experiments, a sample rate of 2.1 GSa/s was obtained by interleaving two 1.05 GSa/s channels; higher sample rates can be achieved by increasing the channel count. These results indicate that a practical integrated photonic ADC, successfully overcoming the electronic jitter bottleneck, is possible today.

The silicon chip described in this work contains the core optical components of the photonic ADC, which is the modulator, wavelength demultiplexers, and photodetectors. This chip is not yet a fully integrated photonic ADC because as the-detection electronics, electronic ADCs for amplitude quantization and post-processing are not integrated. This silicon chip can therefore be viewed as a photonic front-end which functions as a pre-processor and demultiplexer for electronic ADCs. In this capacity, it enables sampling speeds and jitter levels which at the moment cannot be achieved with electronics alone. The next major step would be to put high-speed electronics on the same chip with photonics, which should soon be possible due to rapid advances in the electronic-photonic integration technology.

The main message of this work is that the problem of jitter and comparator ambiguity in high-speed ADCs can be eliminated with the photonic approach thanks to superior jitter properties of mode-locked lasers and the use of optical sampling. It is necessary to emphasize that the low jitter alone does not guarantee accurate analog-to-digital conversion because other imperfections can potentially limit the ADC performance. Such imperfections include noise from photodetectors, RF amplifiers, and individual electronic ADCs, as well as nonlinear distortions from the modulator, photodetectors, and post-detection electronics. It is an enormous challenge to balance the large number of photonic wavelength channels required for high-speed sampling and to reduce imperfections of the electronic detection and post processing to translate the orders of magnitude improvement in jitter into the commensurate improvement in ADC performance. However, it appears that no fundamental obstacles exist on this path. For example, the shot noise limit can be reduced by increasing the input optical power and reducing the optical losses in the system, the RF noise and distortions can be reduced by proper design of the RF subsystem, modulator nonlinearity can be suppressed with linearization or post-compensation, photodetector designs can be optimized for linearity, and so on. This work makes a step towards overcoming these obstacles, and we believe that further steps forward are possible now after the most fundamental obstacle – the aperture jitter – has been removed with the photonic approach.

While the photonic ADC realized in this work is shown on the "Walden chart" (Fig. 1) as significantly outperforming all electronic ADCs, it is important to emphasize that this work reports an experimental investigation rather than a final product and important differences exist between the photonic and electronic data points of Fig. 1. First, the electronic ADCs shown on the Walden chart are either commercially available products or fully functional ADC chips which include internal calibration and error compensation. On the other hand, the results reported in this work were achieved in a laboratory experiment, and although they demonstrate a significant potential of the photonic approach, a substantial amount of work is required to create a finished photonic ADC product. The second difference is that the photonic ADC reported in this work undersamples the signal by a significant factor (about 40). A large fraction of the best-performing electronic ADCs of Fig. 1 also sample below the Nyquist rate, but the factor by which they undersample is smaller (2 or 4). To be truly comparable to the electronic ADCs of Fig. 1, a photonic ADC must have more channels than demonstrated here. In principle, the integration approach pursued in this work makes physical implementation of a many-channel photonic ADC a straightforward task. The challenge is to

#156800 - $15.00 USD Received 19 Oct 2011; revised 1 Feb 2012; accepted 1 Feb 2012; published 8 Feb 2012

balance these channels and compensate for mismatches between them, as it is done in multi-channel electronic ADCs. These are the differences between the photonic and electronic data points in Fig. 1, and while it appears that no fundamental obstacles exist on the way to bringing photonic ADCs closer to a final product with all the required channels, it is necessary to keep in mind that this is still a challenging task.

Appendix: Data points shown in Fig. 1

Blue circles in Walden plot (Fig. 1) correspond to ADCs from Walden's survey of ADCs as of late 2007 [4]. Dark blue circles correspond to ADCs reported since 2007, namely: Nortel, ISSCC 2009 paper: 4.1 bits @ 8 GHz; Nortel, ISSCC 2010 paper [2]: 3.9 bits @ 18 GHz; Rensselaer Polytechnic, JSSC 2010 paper [3]: 3.5 bits @ 10 GHz; Rockwell RAD006: 5.5 bits @ 10 GHz; Teledyne RAD004: 4.5 bits @ 4 GHz; National Semiconductor ADC12D1800: 8.4 bits @ 1.45 GHz; Analog Devices AD9446: 11.6 bits @ 0.17 GHz; Analog Devices AD9460: 12.3 bits @ 0.225 GHz; Texas Instruments ADS5474: 10.5 bits @ 0.45 GHz; Analog Devices AD9467-250: 12.1 bits @ 0.3 GHz; Linear Technologies LTC2217: 12.8 bits @ 0.14 GHz; Linear Technologies LTC2208-14: 11.9 bits @ 0.25 GHz; Linear Technologies LTC2216: 12.8 bits @ 0.14 GHz.

Orange stars in Fig. 1 represent high-performance photonic ADCs mentioned in this article [28,32–34]. The emphasis of this work is on wideband ADCs. Therefore, although some optically-sampled ADCs intended for narrowband operation demonstrated impressive results [35,36], they were not included in Fig. 1 because they cannot be easily scaled to wideband operation.

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